MULTI-THRESHOLD LOW POWER-DELAY PRODUCT MEMORY AND DATAPATH COMPONENTS UTILIZING ADVANCED FINFET TECHNOLOGY EMPHASIZING THE RELIABILITY AND ROBUSTNESS

A Thesis

Submitted to the Faculty

of

Purdue University

by

Avinash Yadav

In Partial Fulfillment of the

Requirements for the Degree

of

Master of Science in Electrical and Computer Engineering

December 2020

Purdue University

Indianapolis, Indiana

THE PURDUE UNIVERSITY GRADUATE SCHOOL
STATEMENT OF THESIS APPROVAL

Dr. Maher E. Rizkalla, Chair

Department of Electrical and Computer Engineering

Dr. Trond Ytterdal

Department of Electrical and Computer Engineering

Dr. John J. Lee

Department of Electrical and Computer Engineering

Approved by:

Dr. Brian King

Head of Graduate Program

"To god, my mummy & papa, my sisters, and my dearest SanR"

- Dedication from the author

"You can't connect the dots looking forward; you can only connect them looking backwards. So you have to trust that the dots will somehow connect in your future. You have to trust in something — your gut, destiny, life, or karma.

Stay hungry, Stay foolish!"

- Steve Jobs, Apple

ACKNOWLEDGMENTS

I would like to thank my thesis advisers, Dr. Maher E. Rizkalla, Dr. John J. Lee, and Dr. Trond Ytterdal for their patience, continued guidance, and providing me the opportunity to contribute to both device and system level in the field of ULSI Design. Although I did not have the privilege to take a course with Dr. Ytterdal, he provided me the time and advice whenever we met and helped increase my knowledge in the field of Circuit Design. Besides, I would also like to thank Dr. Brian King, Sherrie Tucker, Anoop Gopinath, and Rob Meagher for their help and support in my graduate life.

TABLE OF CONTENTS

Page

Page

LIST OF TABLES

Table Page

LIST OF FIGURES

Figure Page

SYMBOLS

μ_n	Mobility of Electrons
μ_n	Mobility of Holes
ϵ_{ox}	Permittivity of Gate Oxide
g	Logical Effort
h	Stage Effort or Fanout
p	Parasitic Effort
d	Normalized Delay
W_N	PMOS Channel Width
W_P	NMOS Channel Width
t_{ox}	Thickness of the Oxide Layer
V_{BS}	Body to Source Voltage
V_{DS}	Drain to Source Voltage
V_{GS}	Gate to Source Voltage
V_{th}	Threshold Voltage
$M1$	Metal Layer 1
WL	Word Line
BL	Bit Line
BL_{br}	Bit Line Bar
Clk	Clock
I_{GS}	Gate to Source Current
I_{DS}	Drain to Source Current
C_L	Load Capacitance
t_r	Rise Transition Delay
t_f	Fall Transition Delay

t_{cd}	Comb Logic Contamination Delay
t_{pd}	Comb Logic Propagation Delay
t_{setup}	Setup time of Flop
t_{hold}	Hold time of Flop
t_{cq}	Clock to Q Delay of Flop

ABBREVIATIONS

ADE	Cadence Virtuoso Analog Design Environment
ALU	Arithmetic and Logic Unit
BTBT	Band to Band Tunneling
ptshell	Synopsys Primetime Command Shell
dcshell	Synopsys Design Compiler Command Shell
lcshell	Synopsys Library Compiler Shell
CPU	Central Processing Unit
DRV	Logical Design Rule Violators
DRC	Design Rule Check
DP	Design Planning
DIBL	Drain Induced Barrier Lowering
DFT	Design for Test
D-FF	D Flip-Flop
DEF	Design Exchange Format
DB	Synopsys Binary Database File
ECO	Engineering Change Order
GIDL	Gate Induced Drain Leakage
mV	Millivolt
nm	Nanometer
ps	Picosecond
INV	Inverter
TT	Typical-Typical (Nominal) Corner
SS	Slow-Slow (Max Delay) Corner
FF	Fast-Fast (Min Delay) Corner

FO4	Fanout of 4 Delay
FO6	Fanout of 6 Delay
STA	Static Timing Analysis
PUN	Pull Up Network
PDN	Pull Down Network
SRAM	Static Random Access Memory
SDC	Synopsys Design Constraints
SRAM	Static Random Access Memory
LIB	Liberty Timing File
LEF	Layout Exchange Format
LVt	Low Threshold Voltage
RVt	Regular Threshold Voltage
SPEF	Standard Parasitic Exchange Format
SLVt	Sub-Low Threshold Voltage
SAIF	Switching Activity Interchange Format
TLUplus	Table Look Up RC File
FEOL	Front End of Line
BEOL	Back End of Line
SoC	System on a Chip
TCL	Tool Command Language
Perl	Practical Extraction and Reporting Language

ABSTRACT

Yadav, Avinash. M.S.E.C.E., Purdue University, December 2020. Multi-Threshold Low Power-Delay Product Memory and Datapath Components Utilizing Advanced FinFET Technology Emphasizing the Reliability and Robustness. Major Professor: Dr. Maher Rizkalla.

In the era of high-speed circuits and systems, CMOS technology has reached its limits. The balance of power, performance, and area trade-off is the base of current digital systems. Industries are designing chips at the cutting-edge technologies using 3nm, 5nm, 7nm, and 10nm processes. These advanced node technologies allow to efficiently direct the flow of electrons making the high-performance low-power devices physically possible. The aforementioned Power Performance Area (PPA) trade-off varies significantly for different applications. Moreover, semiconductor device parameters vary with the process and environmental variations that are modeled under term Process, Voltage, and Temperature (PVT). A satisfactory PVT operating conditions ensure the good behavior of the circuit for the desired application.

In this thesis, we investigated the 7 nm FinFET technology for its delay-power product performance. In our study, we explored the ASAP7 library from Arizona State University, developed in collaboration with ARM Holdings. The FinFET technology was chosen since it has a subthreshold slope of 60mV/decade that enables cells to function at 0.7V supply voltage at the nominal corner. An emphasis was focused on characterizing the Non-Ideal effects, delay variation, and power for the FinFET device. An exhaustive analysis of the INVx1 delay variation for different operating conditions was also included, to assess the robustness.

The 7nm FinFET device was then employed into 6T SRAM cells and 16 function ALU. The SRAM cells were approached with advanced multi-corner stability evaluation. The system-level architecture of the ALU has demonstrated an ultra-low

power system operating at 1 GHz clock frequency. The ALU design introduces an Intellectual Property (IP) characterized by different PVT corners suitable for Low power, machine learning, embedded systems, and other complex computer arithmetic applications. Each of the circuit and system represents significant speedup over planar CMOS technologies and contributes to the field of Ultra Large Scale of Integrated Circuit (ULSI) design.

The 7 nm FinFET device explored as the minimum threshold voltage of 207mV, maximum effective current of 18.26 μA, and maximum power consumption of 14.75 μW with high speed measured via multi-corner simulation. A comparative study between the various advanced technologies was introduced to designate the unique features of the FinFET system technology.

The successful design and simulation of the SRAM cells led to a robust design for the L2/L3 caches that may feature high-performance microprocessors. A complete FinFET CPU integrating more instructions is reserved for future considerations.

1. INTRODUCTION

High performance-low power designs are the basic need of current microprocessors for applications like data centers, scientific researches, machine learning, and artificial Intelligence. Integrated circuits are designed specifically for their application. Data center and scientific Researches need a multi-core multi-threaded microprocessor to exploit parallelism at different levels (instruction, data, and thread) [1] whereas machine learning and artificial intelligence need powerful Application-Specific Integrated Circuit (ASIC) accelerators along with CPU to boost the dynamic, complex, and unique computational power. Computer arithmetic components such as ALU decides the limitations on boosting power. Developing the design from the lowest levels of the circuit to the system level provides a potential improvement in the concurrent power, performance, and area optimization. Modern industry-standard CAD tools run on NP-Complete algorithms to solve this optimization problem with heuristic approaches [2].

Current customized ASICs are set to be the next step in providing AI compute. One such evolving computational unit is Tensor Processing Units (TPU, introduced by Google) [3] that are built specifically for machine learning models. They show significantly less power dissipation than GPUs and CPUs while achieving trillions of operation per second [4]. These hardware accelerators explore the power of circuit design from transistor to system level to achieve exceptional memory bandwidth and computational power. To fulfill this requirement, the highly optimized computer arithmetic and memory components come into the picture. In summary, CPUs, GPUs, and TPUs are becoming more optimized for their purpose. However, the circuit level optimization on sub-nanometer processes for various parameters (supply voltage, power consumption, area, and delay) provides a bound on application selection for implementation.

1.1 Motivation

The Power, performance and area trade-off is the key strategy to market current generation microprocessors. Performance of a processor is judged on the execution time that can be denoted using following equation [5]:

$$ExecutionTime = IC * CPI * T_c$$

where, IC= Instruction Counts;
CPI= Cycle Per Instruction;
T_c*= Clock Period*

Instruction counts and cycle per instruction are two parameters that depend on the architectural specification of any system. To reduce execution time and increase performance these parameters can merely be controlled by using techniques like pipelines and parallelism. These techniques reduce the aforementioned parameters but they also encounter limitations of basic circuit design. For example, increasing pipelining causes sequencing overhead of flip-flops to increase and hence not useful. Moving to the third term of the equation: Clock period T_c or inversely clock frequency is the parameter that defines the performance constraint on any system from a circuit design perspective and states that: How fast a circuit can switch? The only answer to this question is "by designing faster transistors". To achieve this switching speed, advanced transistor processes like 5nm Nano-Sheet Transistors and 7nm FinFETs are developed [6]. They allow circuit designers to optimize a design for power consumption, speed, and area. Keeping this in mind, this thesis presents circuit and system-level designs that are highly optimized for better Quality of Results (QoRs).

1.2 ASAP7 PDK Overview

In the past few decades, Moore's law has resulted in significant improvement in computing performance. The submicron transistor chips are being fabricated using multi-patterning that shows a gesture of immersion lithography limitations. This is

the most challenging phase for design makers [7]. The 7nm ASAP kit provides an access to realistic designs that are not yet accessible from the industry. This library comes with the feature required for transistor-level design and simulation, layout design rule checks, logic synthesis, and placement & routing (APR) [8].

1.3 Custom and Digital Design Methodology

Design Methodology or Design Flow deals with how a design is implemented using multiple steps through different tools [9]. They process the design to get the implementation done most cost-effectively. Every design flow has its limitations. Currently, two types of design flow are considered to be matured to implement the design: Custom Design Flow and Digital Design Flow. Custom Design methodology is used to capture a mixed-signal design that includes transistor-level schematic design, layout optimization, and spice simulation to analyze the behavior of the circuit. Advanced Custom Design Flow uses complex tools such as Cadence Quantus for parasitic extraction for the post-layout simulation that mimics actual process and environmental variation [10]. This ensures the reliability and robustness of the circuit before fabricating it.

The Digital Design Methodology or ASIC Design Methodology or Behavioral Synthesis Design Methodology is the one that specifies the functionality on RTL level using HDLs like System Verilog, Verilog, and VHDL. It is considered as the most popular tool dependent flow that provides freedom of optimizations to the tools, and modern tools use NP-Complete algorithms to solve the implementation problem utilizing a heuristic approach. During the design cycle, the design is processed through multiple verification steps:

- Assertion-based Functional Verification (OVM, UVM, etc.)
- Design for Test Checks (BITs, Scan Chains, etc.)
- Static Timing Analysis (Min/Max Delay, etc.)
- Formal Verification for Logical Equivalence Check
- Physical Verification (LVS, DRC, etc.)

1.4 Proposed Implementation

In this dissertation, the aforementioned library is utilized to assess the capability of 7nm FinFET transistors on circuit and system levels. The analysis started with an NMOS transistor to characterize it for non-ideal IV effects, threshold voltage effects, and leakages present at the subnanometer level. All multi-corner characterizations are performed on Cadence Virtuoso ADE Assembler and Explorer. Further, this characterization is extended on an INV cell where the multi-corner VTC is produced for different PVT conditions. This also includes the delay calculation of a FO4 inverter and introduces a new term called "FO6" delay to achieve equal effective NMOS and PMOS currents [11]. The 6T SRAM cells are well known for providing robust, low power, and high area-efficient caches for microprocessors. This thesis also assesses the capability of a 7nm 6T SRAM cell for its hold margin, writability, and readability. Advanced techniques are also proposed to achieve exceptional writability and readability. Lastly, this thesis presents a high power optimized 32-bit ALU using Design Ware components provided by Synopsys as part of their synthesis tools. To implement the design, a methodology was developed to integrate the tools from Synopsys and Cadence. This involved various industry standard file generation from one tool and use them on another. Completing this task and extracting useful data manually was quite tedious. Hence, scripting languages TCL and Perl are coded for file handling and flow automation. The physical implementation of the ALU is executed on the Cadence Innovus tool with advanced techniques presented further in this thesis. The list of tools used in this thesis are as follows:

- **Custom Design**: Cadence Virtuoso ADE Suite (Explorer & Assembler)
- **Library Development**: Synopsys Library Compiler
- **RTL Synthesis**: Synopsys Design Compiler
- **Formal verification**: Synopsys Formality
- **STA**: Synopsys Primetime
- **Physical Design**: Cadence Innovus

2. NANOMETER DEVICES AND CAD TOOLS

The 7-nm predictive process design kit (PDK) is also known as ASAP7 PDK [8]. This library was developed by Arizona State University in collaboration with Arm Holdings. It models 7nm technology-node based on current industrial assumptions and developed for academic purposes. Hence, it does not possess real design rules that are associated with any foundry for fabrication. However, developers assume EUV lithography for cost-effectiveness and simpler design rules for BEOL and FEOL metal layers. The PDK includes spice models for transistor level modeling, standard cell timing, and physical view for digital design implementation for the parasitic aware design for highly accurate delay calculations. We explored the library to every possible extent and presented designs on the advance node. This dissertation covers from analysis of an NMOS for non-ideal effects to the implementation of datapath elements to present exceptional timing, area, and power QoR numbers.

The library is developed to support the realistic power and performance of various corner models provided in PDK. Table 2.1 shows all possible combinations of BSIM-CMG spice and liberty timing files [12]. Typical-Typical (TT) corner has nominal transistor parameters presented in Section 3.2 at 0.7V supply voltage. Slow-Slow (SS) and Fast-Fast (FF) corners work at 0.63V and 0.77V respectively to model the environmental variation in supply voltage. It also comes with Design rule checks (DRC) and Layout vs. schematic (LVS) files supported by Mentor Caliber. The parasitic aware design is another feature of this library to estimate proper parasitic resistance and capacitance numbers.

2.1 Library Structure

The entire PDK is structured in two parts: transistor-level spice models and standard cell's timing and physical view. The spice models are used to implement transistor-level circuits on Cadence Virtuoso whereas the digital part of the library supports Cadence RTL Compiler (Logic Synthesis) and Cadence Innovus (Physical Design). The timing view comes in liberty nonlinear delay model (NLDM) that uses tables and interpolation to compute the delay in correlation with the delay modeling schemes [12]. In this thesis, a methodology was developed to integrate Synopsys front-end and Cadence backend tools to aggressively optimize using advanced techniques like boundary optimization, ungrouping hierarchies, adaptive retiming, etc. for the ALU design. All optimizations covered multi-corner implementation to propose a robust approach.

Table 2.1.
Transistors and liberty PVT corners description

Transistor	**SLVt**	**LVt**	**RVt**	**SRAM**
SS	slvt_ss0p63v100c	lvt_ss0p63v100c	rvt_ss0p63v100c	sram_ss0p63v100c
TT	slvt_tt0p70v25c	lvt_tt0p70v25c	rvt_tt0p70v25c	sram_tt0p70v25c
FF	slvt_ff0p77v0c	lvt_ff0p77v0c	rvt_ff0p77v0c	sram_ff0p77v0c

2.2 Variability

Variability considers the circuit behavior at different operating conditions [13]. These three sources of variation: Process, Voltage, and Temperature. They are also known as PVT corners. Any designed circuit must be checked on all extreme corners for better yield and robustness. Table 2.1 presents the all possible PVT conditions for transistor's spice and standard cell's timing models. This thesis presents the designs

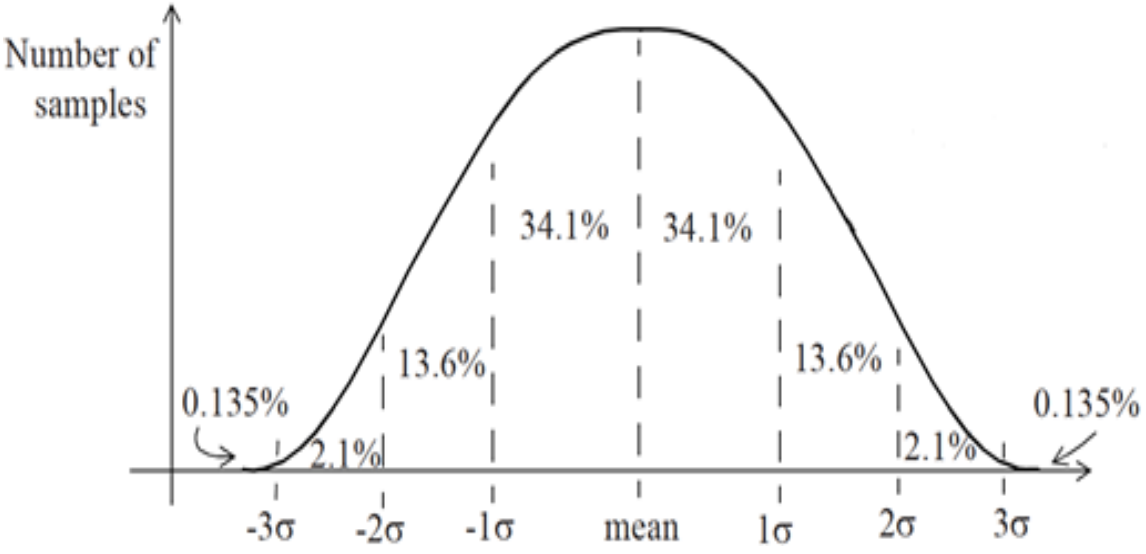

Fig. 2.1. Statistical distribution of process corners.

on the aforementioned operating conditions to consider the variability and reliability in the designs.

2.2.1 Process

Process variation is caused by manufacturing defects and can be divided as Systematic and Random process variation. The systematic process variation can be corrected by improving the manufacturing process but random process variations are modeled using Gaussian Random Variable statistically. Modern standard cell libraries come with the delay variation parameter to assist timing closure at different corners using techniques like On-Chip Variation (OCV) [14]. The 7nm FinFET library comes with multiple corners that are used to create the best or worst timing scenario for STA. Figure 2.1 shows the Normal Distribution function to depict process variation. The deviation from the mean is 3σ on either side. In Static Timing Analysis, the global process variations are modeled statistically using this distribution function.

The fastest corner FF refers to the -3σ point on the horizontal axis whereas +3σ models the slowest corner SS. To perform timing analysis more accurately, the process corners define the precise scenarios on which a design needs to be closed for desirable performance.

2.2.2 Supply Voltage

Supply Voltage used for CMOS transistors was too high in comparison with FinFET devices. The nominal supply voltage for FinFET is 0.7V that changes to 0.77V and 0.63V for FF and SS corners of all multi-threshold cells. Variability also affects the supply voltage due to the tolerance of voltage regulator, static and dynamic IR drops. This makes the nominal voltage to vary for each logic gate present in the design.

2.2.3 Temperature

The temperature on a chip is the sum of the junction and ambient temperature. Variation in temperature affects the mobility and threshold voltage of a transistor (including temperature inversion effect). Any hotspot on the chip also increases the temperature that eventually disturbs the delay of the circuit components and has a strong dependence on spatial power dissipation. Temperatures are picked differently for various application purposes like Military, Space, and Commercial. The library comes with 25°C nominal temperature and can be extremely analyzed on 0°C and 100°C for multi-corner analysis.

2.3 Reliability

A single modern integrated circuit has billions of transistors. At this level, interconnect metals and via structures dominates tiny transistors and hence require equal effort in designing. The gate oxide has shrunk to a few angstroms thickness that is

subjected to the various amount of stress during device operation. Metals and gate oxide materials possess failures called Interconnect and Oxide Wearout respectively. These failures have more importance in subnanometer technologies like 7nm. The mechanism of oxide wear out includes:

- Hot Electron Effect
- Negative Bias Temperature Instability(NBTI)
- Time-Dependent Dielectric Breakdown(TDDB)
- Self Heating Effect(SHE)

If the power supply (VDD) is not scaled properly and the transistor gate length decreases, the generated electric field increases the impact ionization. The electrons generated by this impact ionization can damage the gate oxide. This phenomenon is called Hot Electron Effect [15]. NBTI takes place when the holes get trapped inside the gate oxide due to the electrical stress. FinFET devices are also affected by the Self-Heating Effect. The dielectric at the base of a fin in a Fin-FET device forces the heat flow into the metalization. Self-heating also increases NBTI degradation because more traps are created. Hence, self-heating will significantly increase the chance of electromigration and TDDB failures [16]. Moreover, when a high current flows through a thin wire, it eventually causes a void or hillock on the surface of the metal wire. This issue in interconnects is known as Electromigration [17]. This puts a specification for each metal layer's width to flow current efficiently. Process derating factors are utilized to models the parameters involved in ensuring the reliability of the device.

2.4 Layout Design Rules

PDK utilizes a 1nm grid to draw the standard cell's layout [8]. It supports drawing fins manually but can be copied as they occupy the same area in every cell. This helps to produce equal height standard cells. SRAM cells have different design rules and follow the same fin pitch in the entire layout [18]. These rules are much tighter than

usual standard cell rules to provide a dense SRAM array. For this library, the actual design rules are shown in Table 2.2. The fins have a width of 7nm and spacing of 27nm [11].

Table 2.2.
Width and pitches for 7nm FinFET layers.

Layer	**Drawn Width (nm)**	**Pitch** (nm)
Fin	7	27
Active	16	108
Gate	20	54
LISD	24	54
VIA0-VIA3	18	25
M1-M3	18	36
M4 & M5	24	48
VIA4 & VIA5	24	34
M6 & M7	32	64
VIA6 & VIA7	32	45
M8 & M9	40	80
VIA8	40	57

2.5 Standard Cell Physical Views

The physical library is used as the input to the physical design tool that comes in form of Layout Exchange Format (LEF) for the Cadence Innovus tool [19]. In general, the physical library of any technology contains the following necessary components:

- Technology File in tech LEF or .tf format
- Table Look Up RC file or Interconnect technology file
- Standard Cell Layout and Abstract Views

The .tf contains all the physical rules related to a specific technology [20]. It has rule defined for all metals and vias comes with the technology that includes the min width, min spacing, pitch, default width, and min area of each layer. It also specifies the colors of each physical component with varying intensity of R, G, and B. Same information also comes with the tech LEF file. An example of a metal "M1" specification is shown below:

```
LAYER M1
  TYPE ROUTING ;
  DIRECTION VERTICAL ;
  PITCH 0.144 ;
  WIDTH 0.072 ;
  SPACING 0.072 ;
  AREA 0.010656 ;
  SPACING 0.072 RANGE 0.144 4.000 ;
  PROPERTY LEF58_PITCH "PITCH 0.144 FIRSTLASTPITCH 0.180;" ;
  PROPERTY LEF58_EOLKEEPOUT "EOLKEEPOUT 0.073 EXTENSION 0 0 0.124 ;"
  PROPERTY LEF58_CORNERSPACING "CORNERSPACING CONVEXCORNER
  CORNERONLY 0.040 WIDTH 0.072 SPACING 0.072 ;" ;
OFFSET 0.0 ;
END M1
```

Resistance and capacitance values are picked from the TLU plus file to calculate the actual delay through the specific metal layer [21] [22]. For this purpose, the values of resistance for each metal layer are defined depending upon the metal width. Standard cell layouts are abstracted to have less information inside it and hence it has merely pin location and name utilized during the place and route step in physical design. This physical view of the cell is called CELL View or Abstract View in physical design terminology [19]. Below is the description of an INVx1 cell in the low threshold voltage flavor. The origin of the cell is 0,0 that means it starts from the origin, Similarly the metal M1 shapes are defined using coordinates.

```
MACRO INVx1_ASAP7_75t_L
  CLASS CORE ;
  ORIGIN 0 0 ;
  FOREIGN INVx1_ASAP7_75t_L 0 0 ;
  SIZE 0.648 BY 1.08 ;
  SYMMETRY X Y ;
  PIN A
    DIRECTION INPUT ;
    USE SIGNAL ;
    PORT
      LAYER M1 ;
        RECT 0.072 0.504 0.312 0.576 ;
        RECT 0.072 0.9 0.22 0.972 ;
        RECT 0.072 0.108 0.22 0.18 ;
        RECT 0.072 0.108 0.144 0.972 ;
    END
  END A
  PIN VDD
    DIRECTION INOUT ;
    USE POWER ;
    SHAPE ABUTMENT ;
    PORT
      LAYER M1 ;
        RECT 0 1.044 0.648 1.116 ;
    END
  END VDD
  PIN VSS
    DIRECTION INOUT ;
    USE GROUND ;
```

```
    SHAPE ABUTMENT ;
    PORT
      LAYER M1 ;
        RECT 0 -0.036 0.648 0.036 ;
    END
  END VSS
  PIN Y
    DIRECTION OUTPUT ;
    USE SIGNAL ;
    PORT
      LAYER M1 ;
        RECT 0.376 0.9 0.576 0.972 ;
        RECT 0.504 0.108 0.576 0.972 ;
        RECT 0.376 0.108 0.576 0.18 ;
    END
  END Y
END INVx1_ASAP7_75t_L
```

The Layout of the INVx1 cell is shown below in Layout View. This view depicts all the FEOL layers and their shapes that were used to generate the layout of the inverter cell. The layout can be elaborated using the design rules defined in Table 2.1.

2.6 Delay Modellings

To calculate the delay efficiently, tools like Design Compiler and Primetime need three things: input transition, RC network, and the load capacitance. An ideal model calculates the same delay as the spice simulation does at the output of the driver and the input of each receiver. The aim is to calculate the delay through the timing arc of

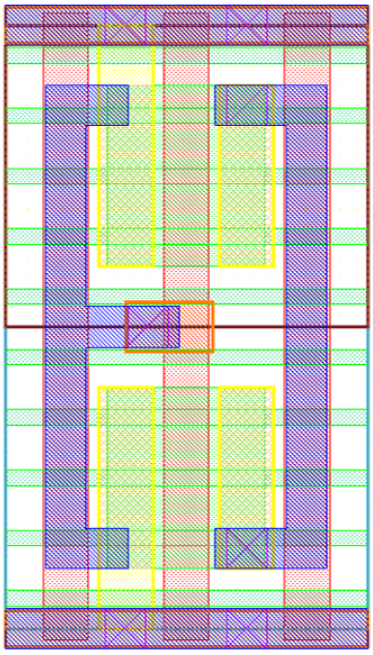

Fig. 2.2. Layout of 7nm FinFET inverter cell.

the cell using input transition and output load. In Liberty files, the delay is presented in various formats using two delay models: Non Linear Delay Model (NLDM) and Composite Current Source Models (CCS) [23]. The ASAP7 library provides liberty files in both NLDM and CCS formats. The NLDM liberty files contain delay in form of a table lookup format shown as following:

```
cell_rise (delay_template_7x7_x1) {
   index_1 ("5, 10, 20, 40, 80, 160, 320");
   index_2 ("0.72, 1.44, 2.88, 5.76, 11.52, 23.04, 46.08");
     values ( \
   "5.24229, 7.7059, 12.5427, 22.1258, 40.998, 78.7789, 154.412",
   "6.51537, 8.97441, 13.7234, 23.2133, 42.2041, 79.9212, 155.651",
   "8.47472, 11.5102, 16.3901, 25.7893, 44.5842, 82.435, 158.021",
   "11.3152, 15.2242, 21.3684, 31.1729, 50.1506, 87.8989, 163.351",
   "15.452, 20.6384, 28.7201, 41.1577, 60.8187, 98.6121, 174.247",
```

```
    "21.9571, 28.6233, 39.2669, 55.6909, 81.0657, 120.103, 195.528",
    "31.9914, 41.0045, 55.0162, 76.5121, 109.767, 160.399, 238.709"
      );
}
```

2.7 Logical Design Rules

Logical Design Rules reflects technology specific limitations that the design must meet to achieve indented functionality [12] [24]. They are specified in logical libraries for each cell. While synthesizing any design advance libraries specify the default values for the synthesis process and generate the gate-level netlist based on that. Typically, design rule constraints contain input transition, load capacitance, and fanout for a cell [25]. Yet additional logical design rules can be specified manually to achieve the desired performance. Tools make sure not to violate the design rules in order to complete optimization constraints. Optimization constraints are described in Section 6.4.1. The utilized logical design rules for the various drive of multi-threshold inverter cells are tabulated in further subsections.

2.7.1 Max Transition

The maximum transition time is a logical design rule constraint that limits the transition value accepted by the input pin of the cell.

```
max_transition : 320;
```

2.7.2 Max Fanout

The maximum output fanout limits the cells to drive the specific number of the cells at the output. Driving large results in large output load capacitance which again causes the cell delay and the output transition to get worst. This can either

cause functionality failures or large short circuit power dissipation. The 7nm FinFET library uses the default fanout number as 1 for all the cells..

```
default_fanout_load : 1;
```

2.7.3 Max Capacitance

The maximum capacitance is the value of the max output load capacitance that the cell can drive. It is mentioned in the library as below:

```
max_capacitance : 368.64;
```

3. FINFET TRANSISTOR CHARACTERIZATION

The rapidly growing electronic industry presented new multi-gate transistors to scale down the device to the sub-nanometer regime. This was possible due to technological advancement in the past few decades that achieved astonishing speed [26]. Planar CMOS devices have fundamental material and process technology limits and exhibit challenging issues like leakage power, supply voltage, and variability. Moreover, shrinking planar CMOS to 10nm and below is difficult due to non-ideal IV effects and realistic manufacturing limits. Non-planar transistor and its variant devices show great potential in manufacturability, package density, and device-stability [27]. FinFET devices, which was proposed as double-gate device, have decades of research and after long ignorance from industries, they are adopted as a standard device for integrated electronics. This kept Moore's law alive [28].

This thesis presents data from 7nm FinFET transistors and describes how the aforementioned challenges are mitigated in FinFET transistors with experimental results. The results include multi-corner simulation with multiple threshold voltage flavors as defined in Section 2.1.

3.1 NMOS Characteristics

This section presents DC characteristics of nMOS LVt transistor in all corner. Figure 3.1 shows the schematic of the test bench for variable sweeping. The I_{ds} vs. V_{ds} for every 0.1V increment in V_{gs} and I_{ds} vs. V_{gs} are shown in Figure 3.2 and Figure 3.3. The gate capacitance (C_{gg}) has significant importance in delay calculation of any circuit and is is the sum of gate to source (C_{gs}), gate to drain (C_{gd}) and gate to body (C_{gb}) capacitance. Figure 3.4 shows gate capacitance for different values of V_{gs}.

$$C_{gg} = C_{gs} + C_{gd} + C_{gb} \tag{3.1}$$

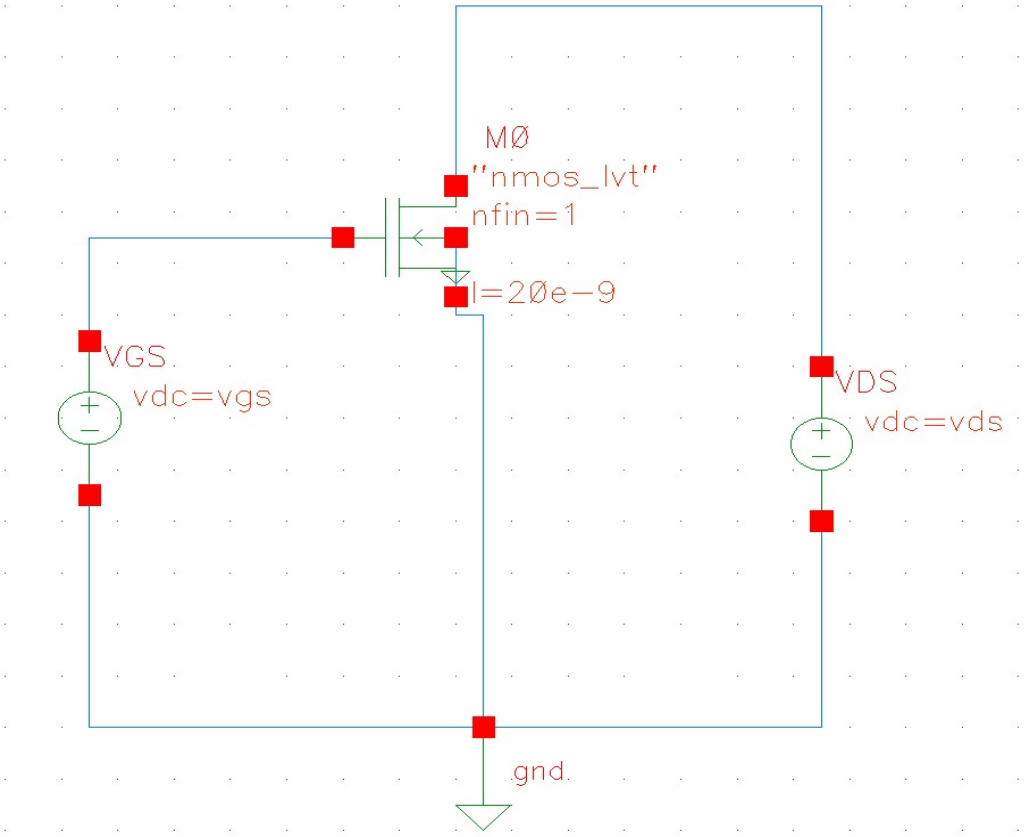

Fig. 3.1. NMOS LVt schematic.

3.2 Multi-threshold Parameters

Table 3.1 compares the threshold voltage (V_{th}), drain current (I_{ds}), gate capacitance (C_{gg}) and dc power with different values of V_{gs} and V_{ds} for TT transistors available in the library. The simulation was performed on ADE Explorer by saving the dc operating point for every Vt cell.

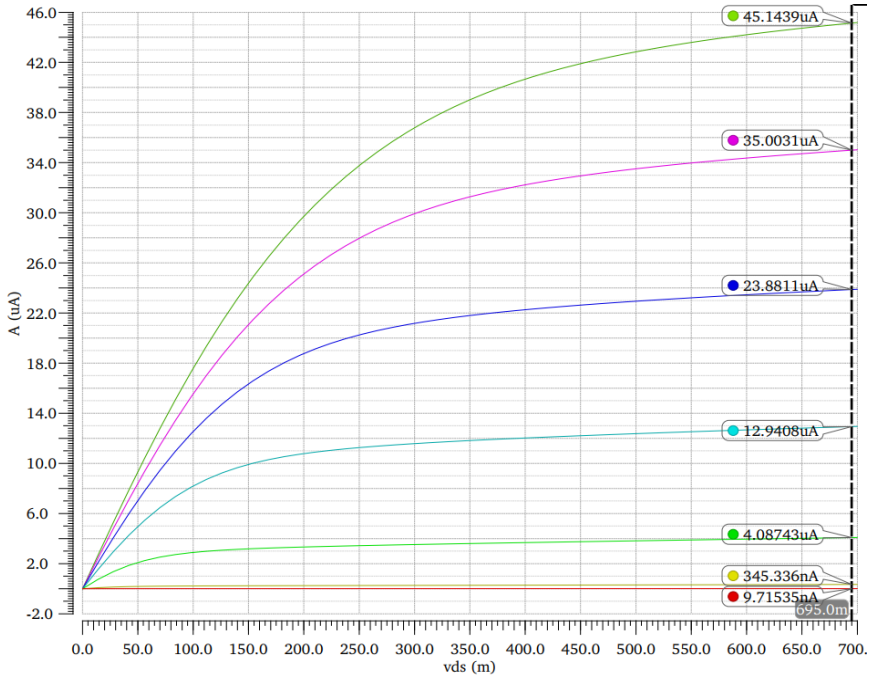

Fig. 3.2. I_{ds} vs. V_{ds} for TT corner.

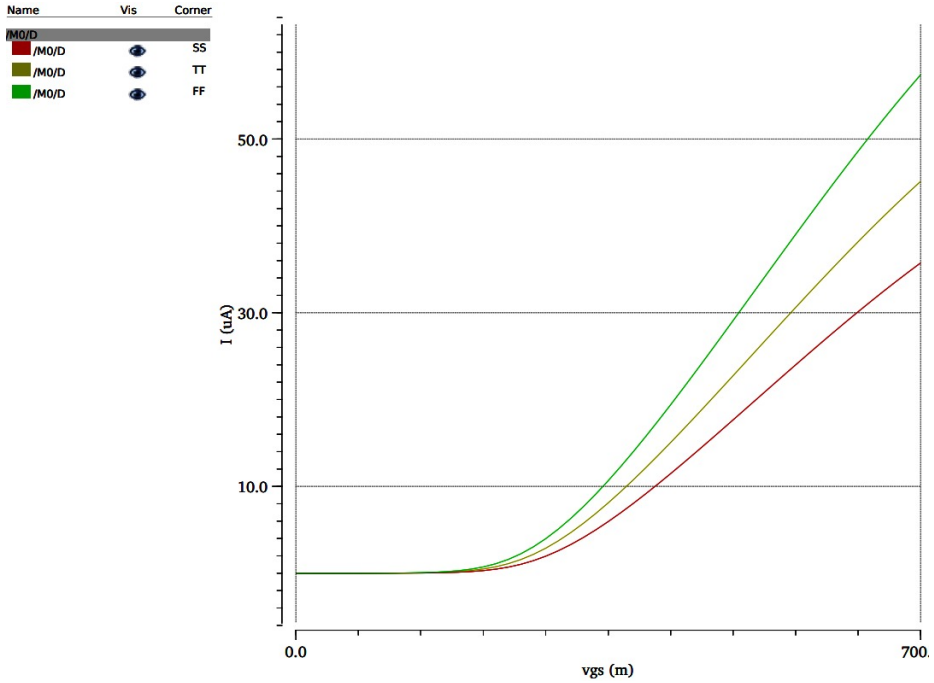

Fig. 3.3. I_{ds} vs. V_{gs} in all three corners.

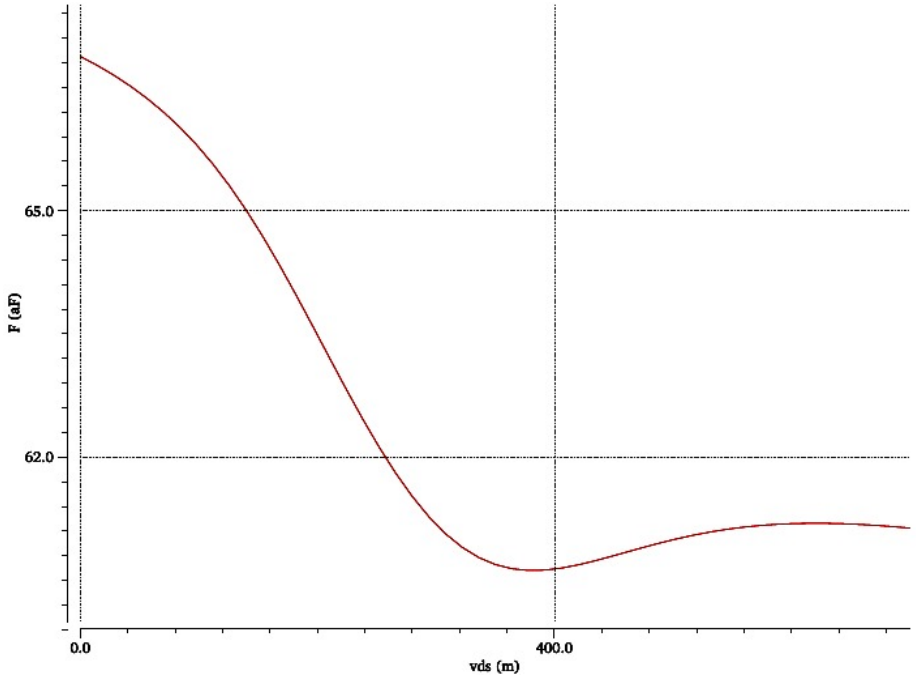

Fig. 3.4. Gate capacitance of NMOS.

Table 3.1.
Comparison of V_{th}, I_{ds}, C_{gg}, and power

Transistor	I_{ds} (uA)	C_{gg} (aF)	V_{th} (mV)	**Power (uW)**
SLVt: TT	50.697	60.47	207	35.42
LVt: TT	45.143	50.11	267	31.5
RVt: TT	37.76	40.29	327	26

3.3 Leakage

Leakage current flows when the chip is not switching and aggressively limits the number of the transistor can be integrated on the chip. Before 90nm, the leakage power was negligible as compared to dynamic power. However, as the process node reduced to a subnanometer, the leakage significantly increased and contributes to one-third of total power consumption. The leakages can be categorized into three parts: subthreshold leakage, gate leakage, and junction leakage. Collectively, these leakage components cause electrons to leak through the ground during the cut-off mode. Individually, subthreshold leakage causes the thermal emission of electrons due to Drain Induced Barrier Lowering (DIBL) [29]. It affects the dynamic circuits and DRAMs as they store charge on capacitance. Gate leakage is a quantum mechanical tunneling (Fowler-Nordheim tunneling and direct tunneling) through the extremely thin (15-20 angstrom) gate oxide [30]. Junction leakage is due to the current in reverse p-n junction formed by source/drain and the substrate of a transistor. The 7nm FinFET tratsitor model was developed under BSIM-CMG (common gate model) and is the industry's first FinFET compact model [31]. The spice model straight-forward assumes the technology trend presented in [32], [33], [34], and [35] to derive the values from BSIM-CMG models based on historical technology trends.

The subthreshold leakage comes into the picture when the transistor is weakly inverted i.e., $V_{gs} < V_{th}$ and it increases with V_{ds} due to the DIBL effect. In the subthreshold regime, the current is measure in the semilog scale and the inverse of

Table 3.2.
Comparison of subthreshold slope

Transistor	**S(mV)/decade**
SLVt: TT	62.96
LVt: TT	62.60
RVt: TT	62.38

the slope of the line is called Subthreshold Slope (S). It gives an idea about the amount of drop in the gate voltage required to reduce the leakage current. The 7nm FinfET BSIM-CMG models presents the subthreshold equation in [31]. Figure 3.6 depicts the leakage power consumption of low threshold voltage cells for multiple corners. CMOS devices had shown a subthreshold slope of 90mV/decade that was improved by Silicon-on-insulator devices up to 78mV/decade. The subthreshold slope for FinFET devices are shown in Figures 3.5 and Table 3.2 presents the comparison of the same among different threshold voltages. Similarly, the leakage current and power are compared in Table 3.3 for multi-corner LVt cells.

Table 3.3.
Comparison of leakage current and power for LVt cell at V_{gs} =0V

Transistor	I_{off} **(pA)**	P_{off} **(pW)**
SS	162.01	5.62
TT	276.22	9.28
FF	424.94	13.80

3.4 Layout

The layout of the P-type FinFET transistor is shown in Figures 3.7 and 3.8. Figure 3.7 shows the N-well, active region, and fins according to the design rule shown in

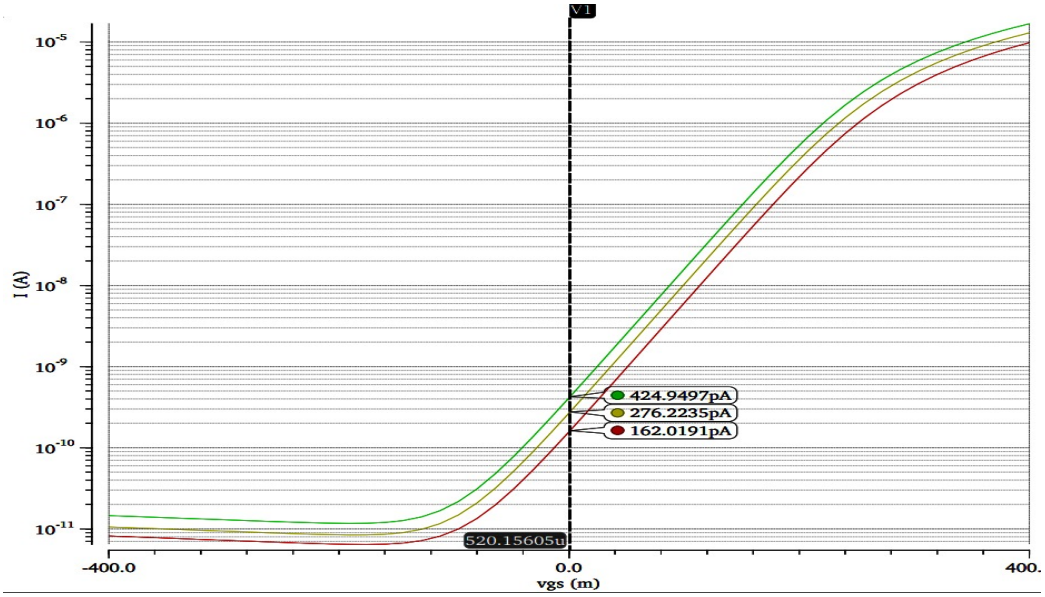

Fig. 3.5. I_{off} of LVt cells on SS, TT, and FF process corners.

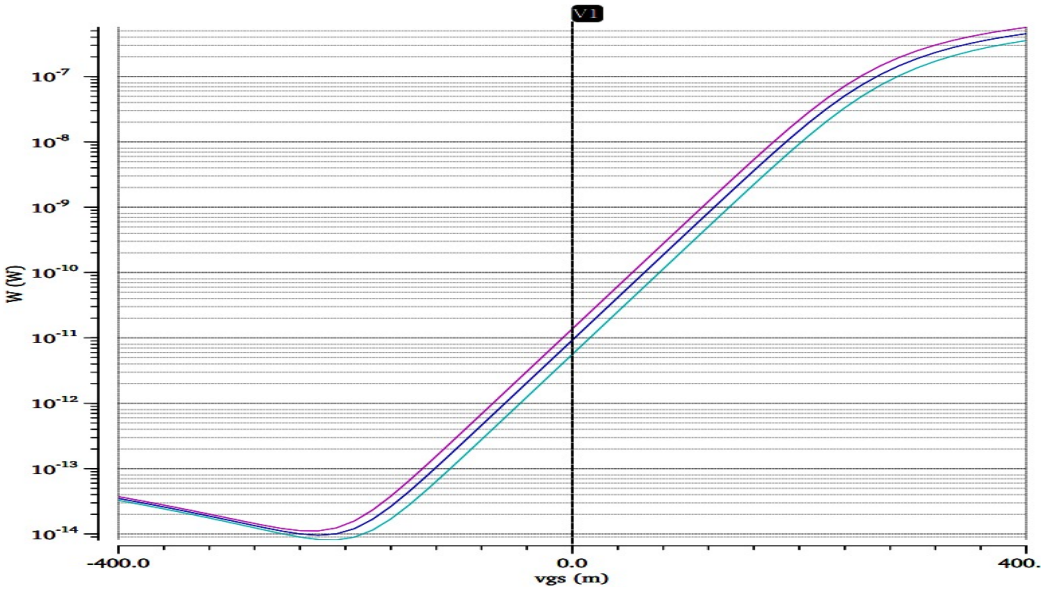

Fig. 3.6. Power of LVt cells on SS, TT, and FF process corners.

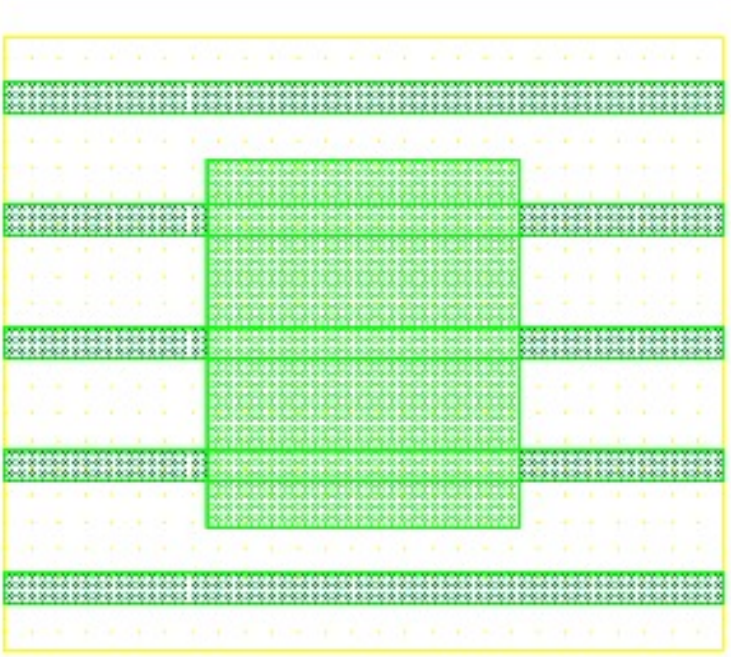

Fig. 3.7. PMOS Layout: Well, Fins, and Active (drawn).

Table 2.1. All the drawn fins are of 7nm width and 27nm pitch as shown in the figure. The poly gate is drawn above the active region to form the transistor and later it is connected to LISD form shape to connect upper metal wires. Similarly, N-type FinFET can be drawn using the rule defined [11].

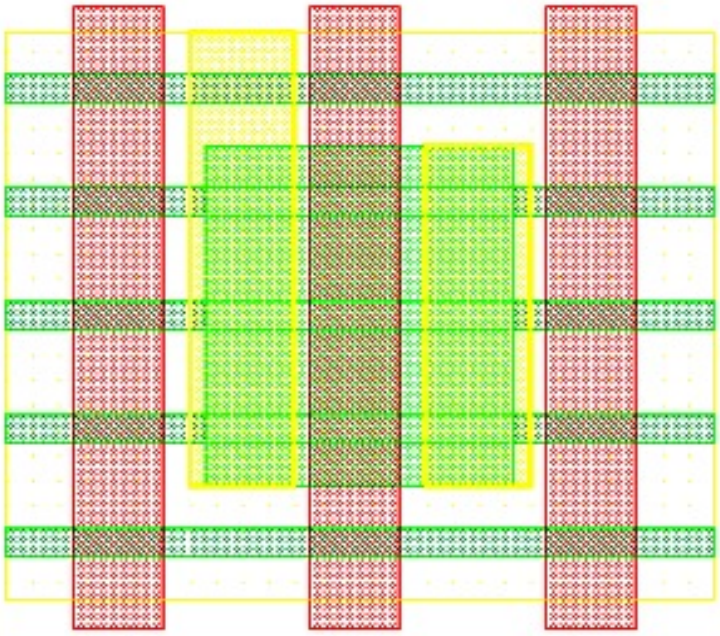

Fig. 3.8. PMOS Layout: Poly gates forming transistor.

4. DELAY AND POWER ANALYSIS

Inverter cell delay is considered as a delay metric in terms of "fanout-of-4 delay" to normalize the process technology. The FO4 delay is the delay through an inverter cell seeing output load capacitance as the sum of four identical inverter's input pin capacitance. The FO4 metric was unchanged for almost all CMOS processes. Advanced FinFET cells do not require the balancing widths and show an equal effective current for NMOS and PMOS transistors. Hence, it introduces the optimal delay at the fanout-of-6 (FO6) delay. Moreover, equal rise and fall transition can be achieved for the clock inverters, unlike CMOS clock repeaters.

The propagation delay is one of the most crucial performance parameters in digital circuit design that requires complex timing models for accurate estimation. Spice models the transistor parameters and are used for the delay computation. In some of the models, the RC circuit approach is used to calculate the delay of the gate. Some of the models are linear delay model, nonlinear delay model, and composite current source model. The linear delay model is based on logical effort (g), electrical effort or fanout (h), and the parasitic delay (p). Normalized delay (d) in the linear delay model is expressed as:

$$d = gh + p$$

The nonlinear delay models add the effect of input transition to the output load capacitance of the linear delay model. Depending upon the polarity of input transition, the propagation delay is calculated separately for the rise and fall transitions. All the pre-calculated values are stored in form of the table look-up format inside the liberty timing files. As the feature size shrunk, the effective metal interconnects resistance started showing highly inaccuracy. Further, to avoid the limitations of NLDM assuming the output load purely capacitive and ignoring the resistance of the inter-

connect, the composite current source (CCS) model is developed. CCS timing model provides additional accuracy by expressing the drivers as a voltage dependent current source. The output DC current is integrated to find the voltage in terms of time into an RC network. The energy of any system can be minimized for the specific desired performance. The power consumption in any logic gate can be broadly classified into two components: Dynamic/Active Power and Static/Leakage Power. Active power is consumed when the logic gates are switching and leakage power is consumed when the logic ages are on standby mode. There are different approaches to model power for the logic gate. The NLDM models store the power numbers in form of a table look-up for different input slope and output capacitance. The following equations show the various powers:

$$P_{static} = V_{DD} * I_{leak}$$

$$P_{dynamic} = P_{transient} + P_{switching}$$

This chapter introduces the model for the evaluation of the transient response, propagation delay, and power consumption for the FinFET inverter cell. An exhaustive multi-corner dc analysis of the inverter cell is also mentioned in the further section that models the sub-nanometer effects. Based on the analysis the experimental results are compared for different threshold voltage cells.

4.1 INV Cell DC Analysis

Figure 4.1 shows the schematic of an inverter cell created on Virtuoso Schematic Editor for single fin LVt NMOS and PMOS transistors. First, the dc analysis was performed to plot the voltage transfer characteristic of the INV cell. This analysis was also used to plot other parameters of each transistor. Figure 4.2 depicts the voltage transfer characteristic of the inverter cell on the TT corner with 0.7 supply voltage. In the later Figures from 4.3 to 4.5, the static power consumption is shown for NMOS and PMOS respectively. Table 4.1 describes the low threshold voltage inverter parameter comparison for the different corners.

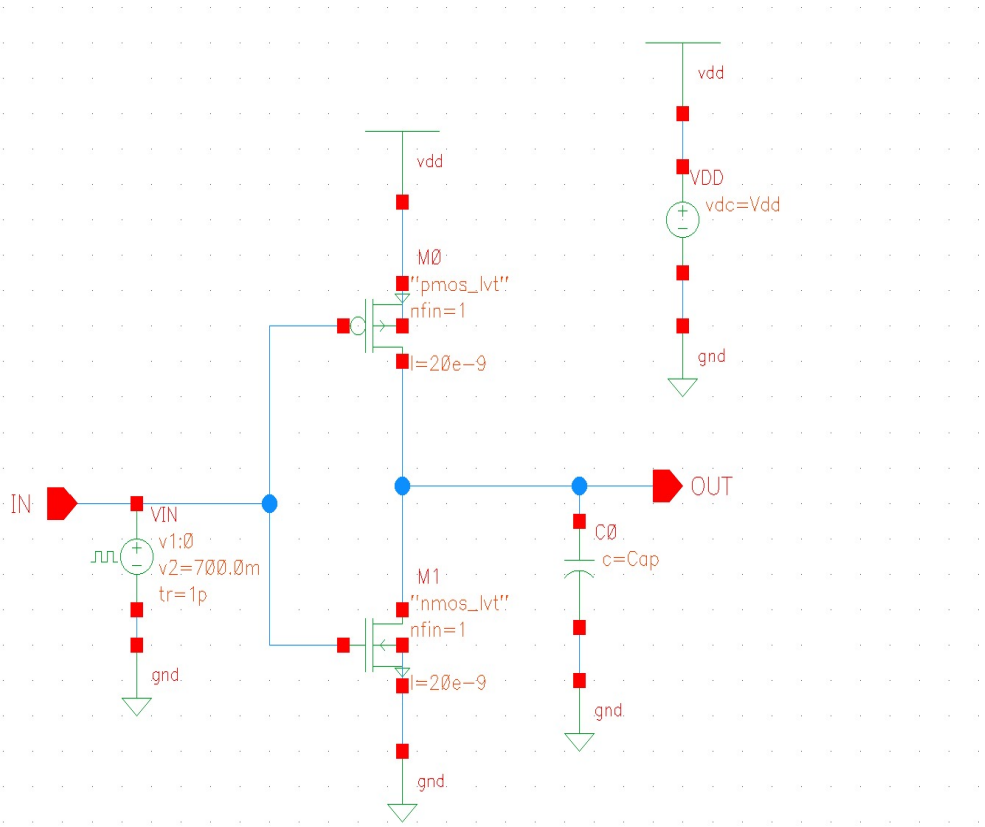

Fig. 4.1. INVx1 LVt schematic

Moreover, inverter parameters threshold volatge (V_{ht}), gate capacitance (C_{gg}), nmos current (I_n), pmos current (I_p) and dc power (P_{dc}) is compared exhaustively multi-corner for each threshold voltage inverter cell i.e, SLVt, LVt, and RVt. Table 4.7 and 4.8 show the variation in aforementioned parameters for same voltage and temperature for NMOS and PMOS respectively for all threshold voltage transistors.

4.2 INV Transient Analysis

Transient analysis is the most fundamental way of delay calculation. It allows us to develop a physical model of a circuit and write the output voltage as the function of input voltage and time. A typical definition of delay is the time taken from 50%

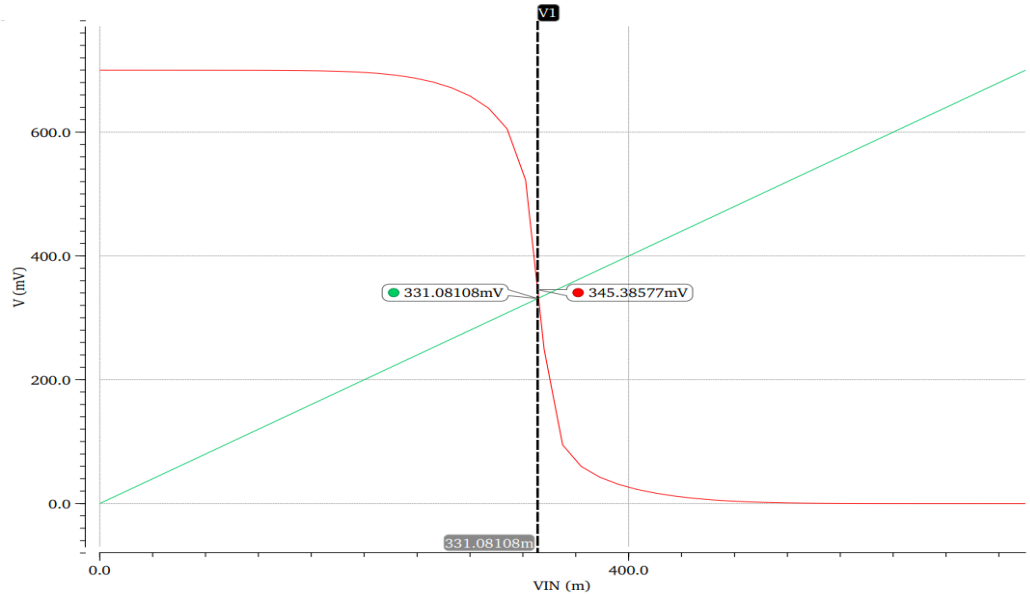

Fig. 4.2. VTC INXx1 TT LVt cell

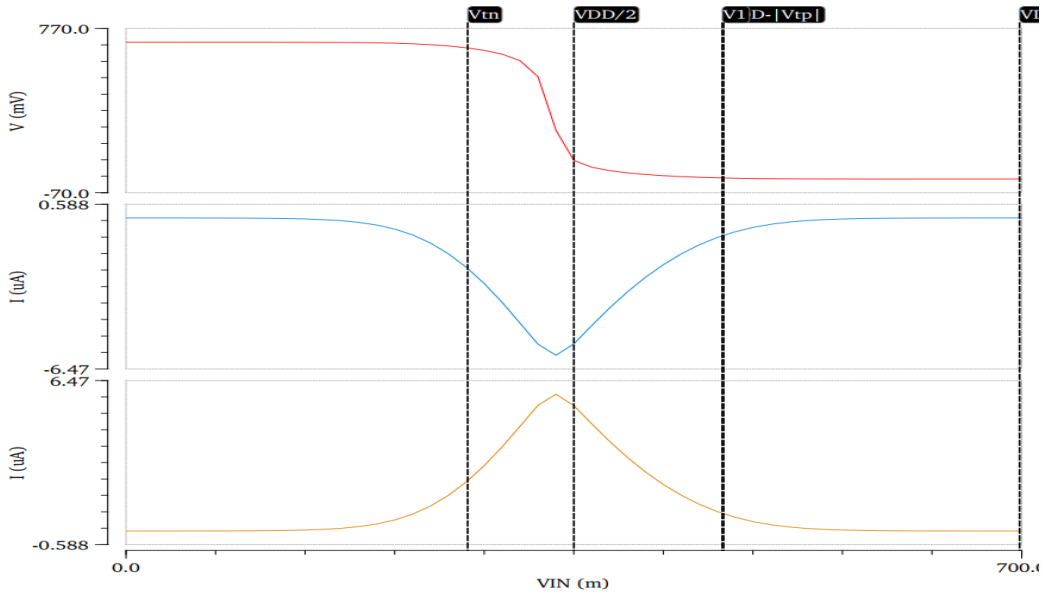

Fig. 4.3. I_{ds} INXx1 TT LVt cell

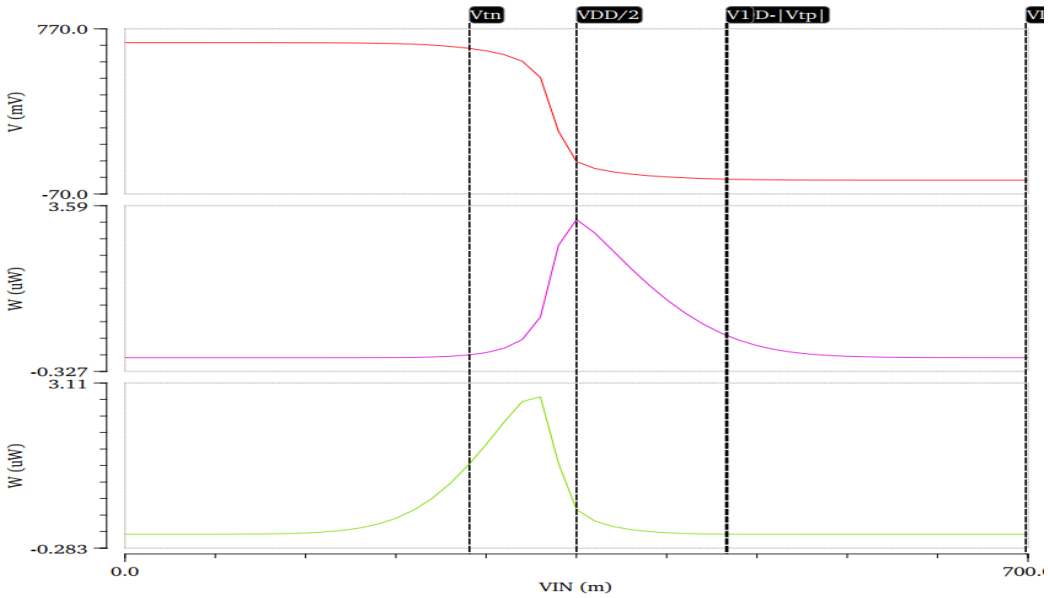

Fig. 4.4. Power INXx1 TT LVt cell

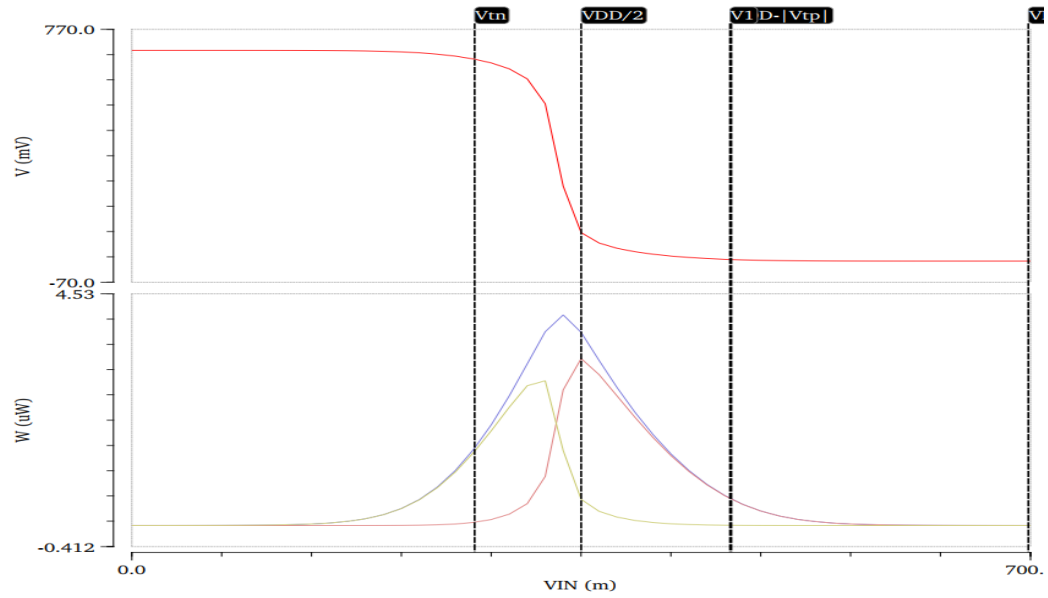

Fig. 4.5. Total Power INXx1 TT LVt cell

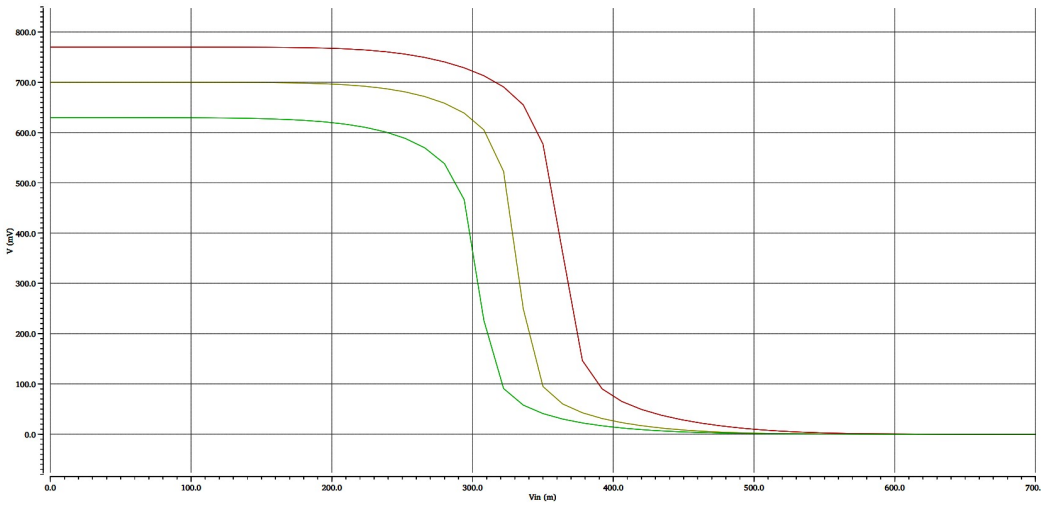

Fig. 4.6. INVx1 LVt multi-corner VTC.

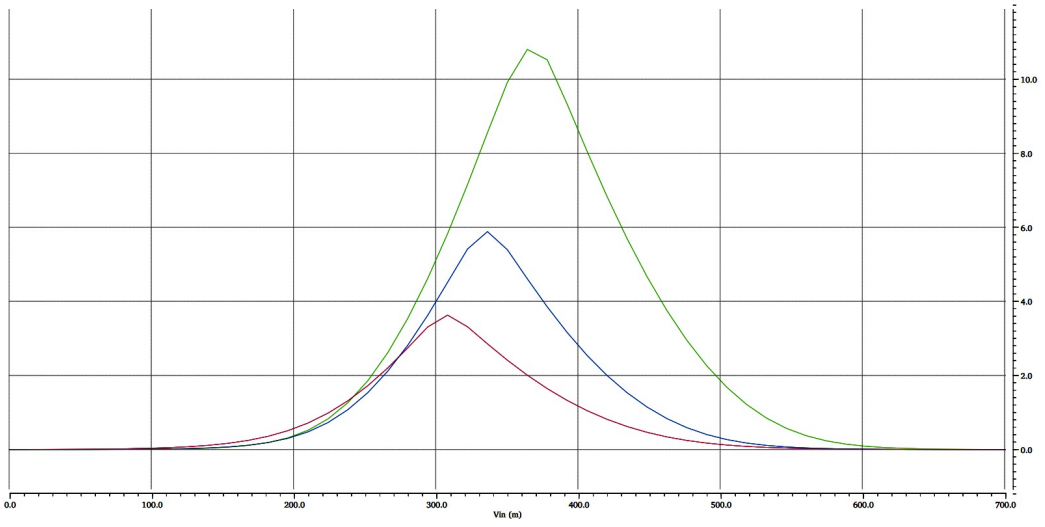

Fig. 4.7. INVx1 LVt multi-corner I_n.

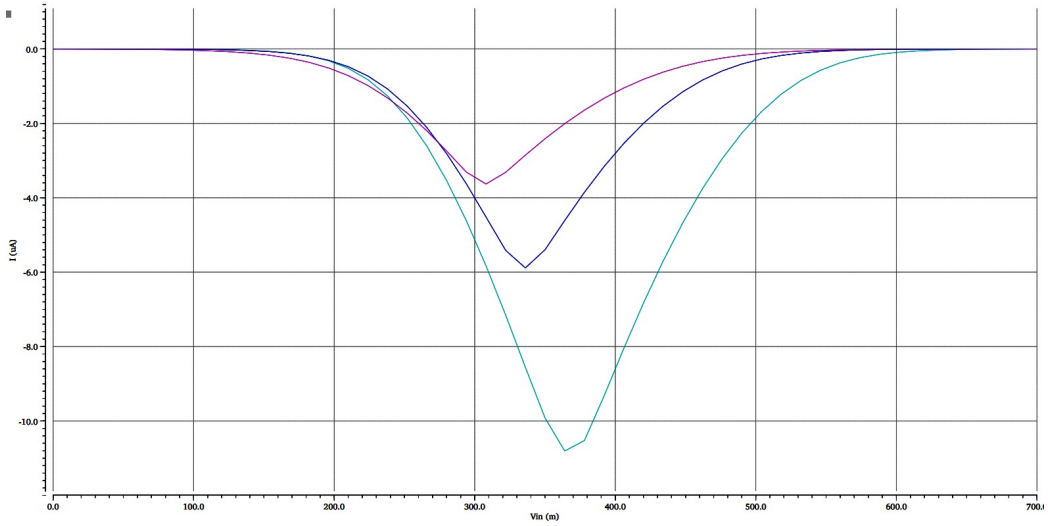

Fig. 4.8. INVx1 LVt multi-corner I_p.

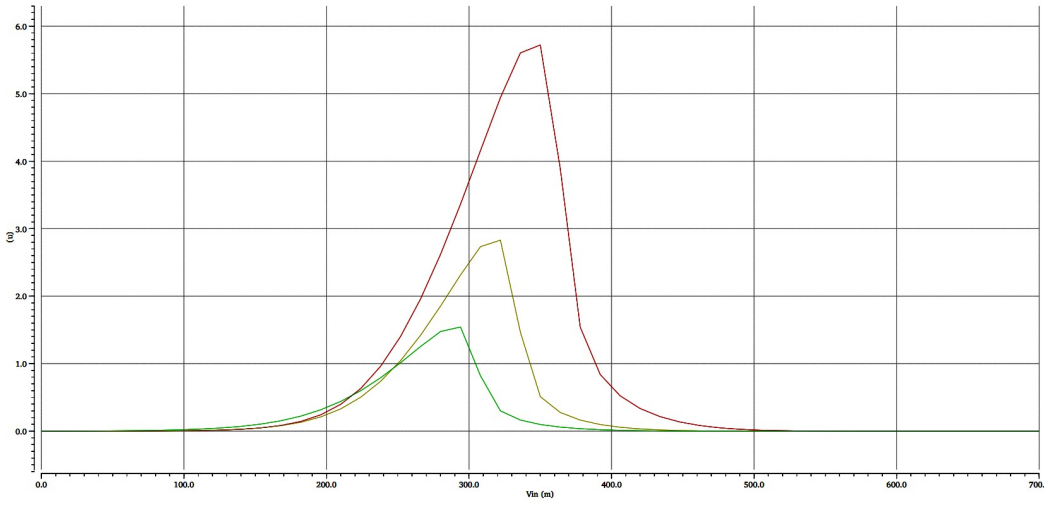

Fig. 4.9. INVx1 LVt multi-corner DC P_n.

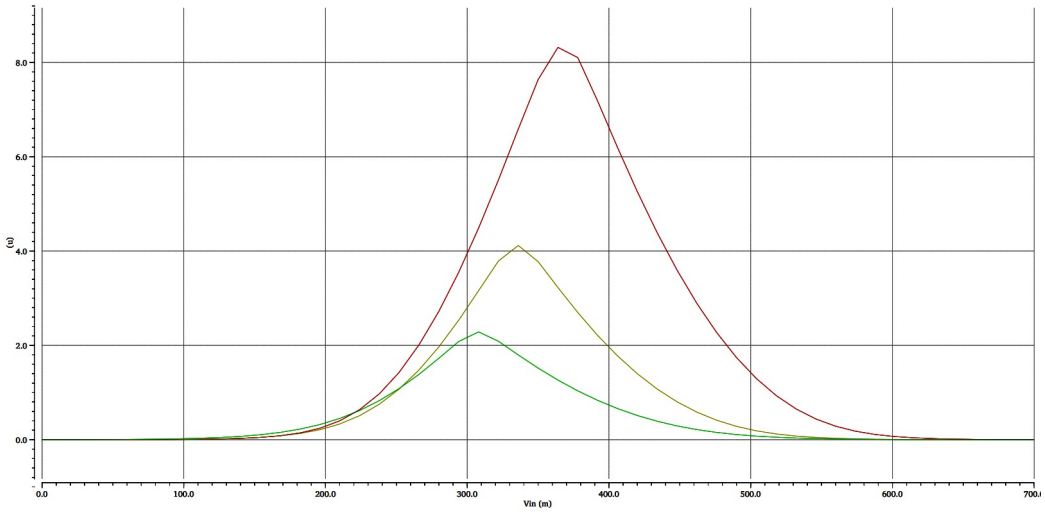

Fig. 4.10. INVx1 LVt multi-corner DC P_p.

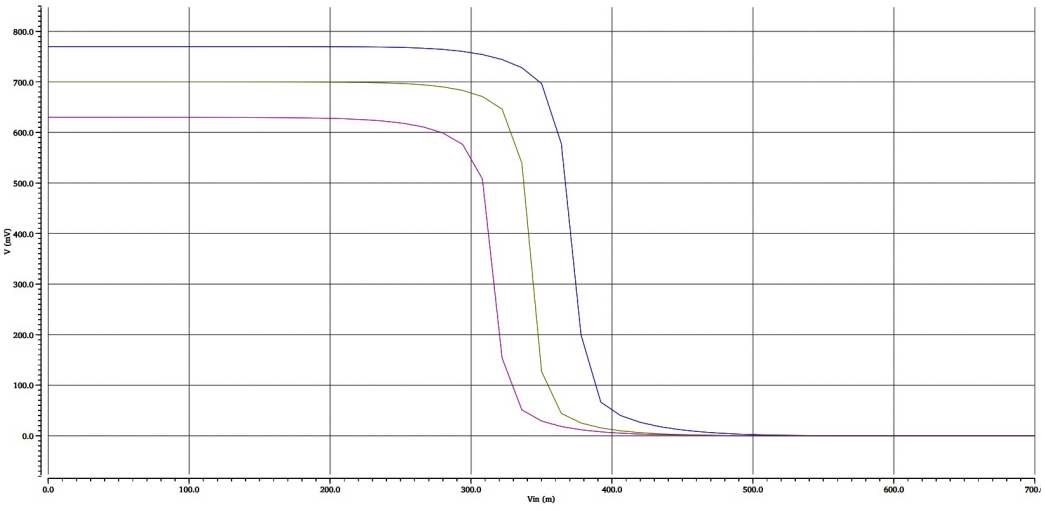

Fig. 4.11. INVx1 RVt multi-corner VTC.

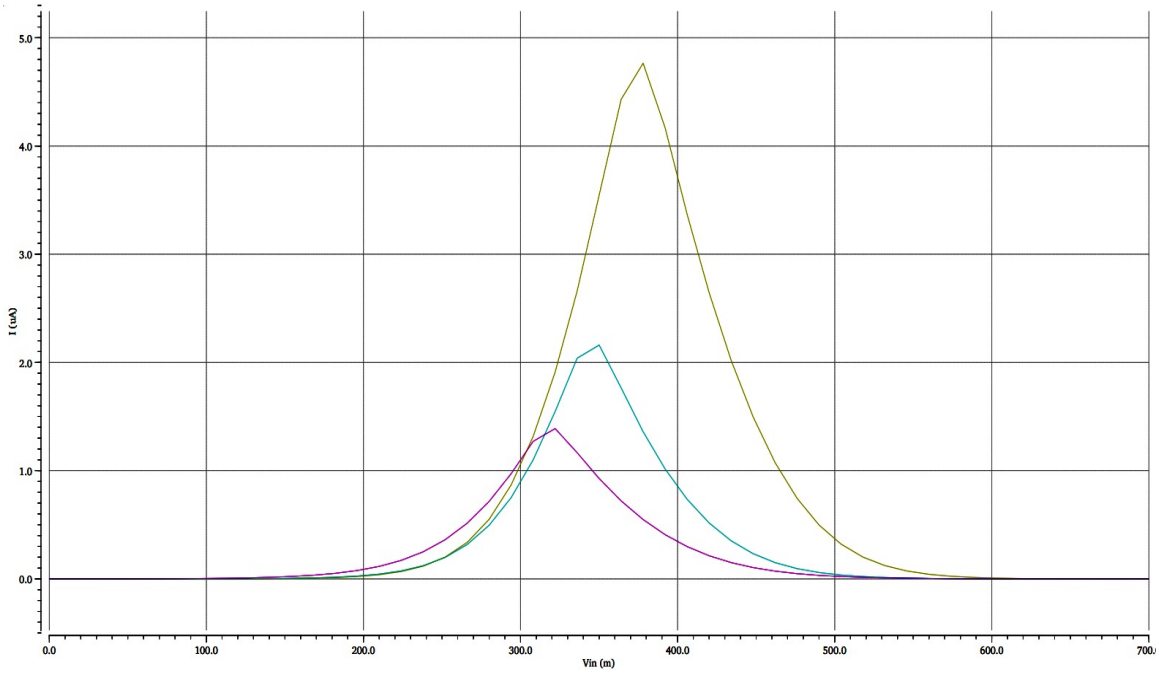

Fig. 4.12. INVx1 RVt multi-corner I_n.

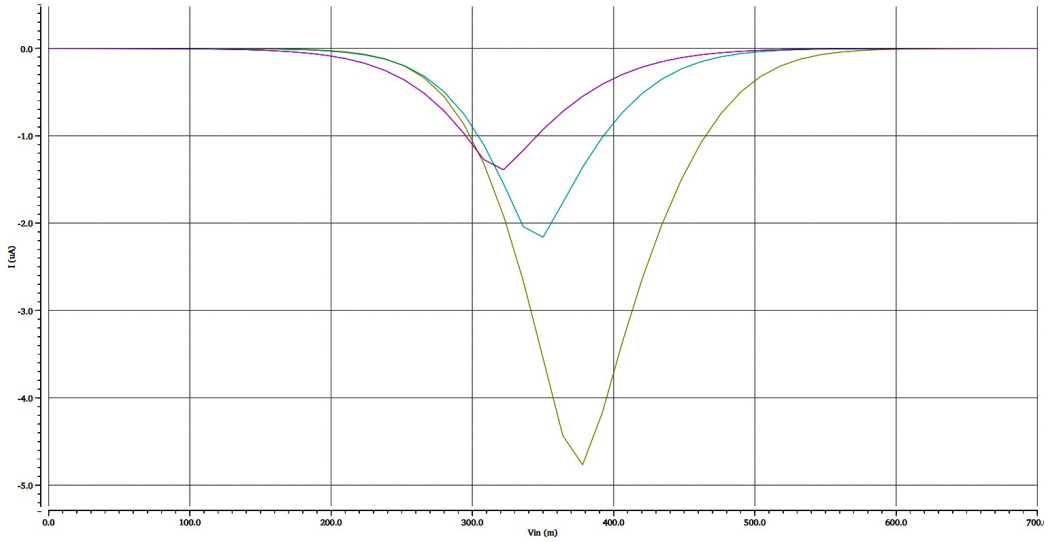

Fig. 4.13. INVx1 RVt multi-corner I_p.

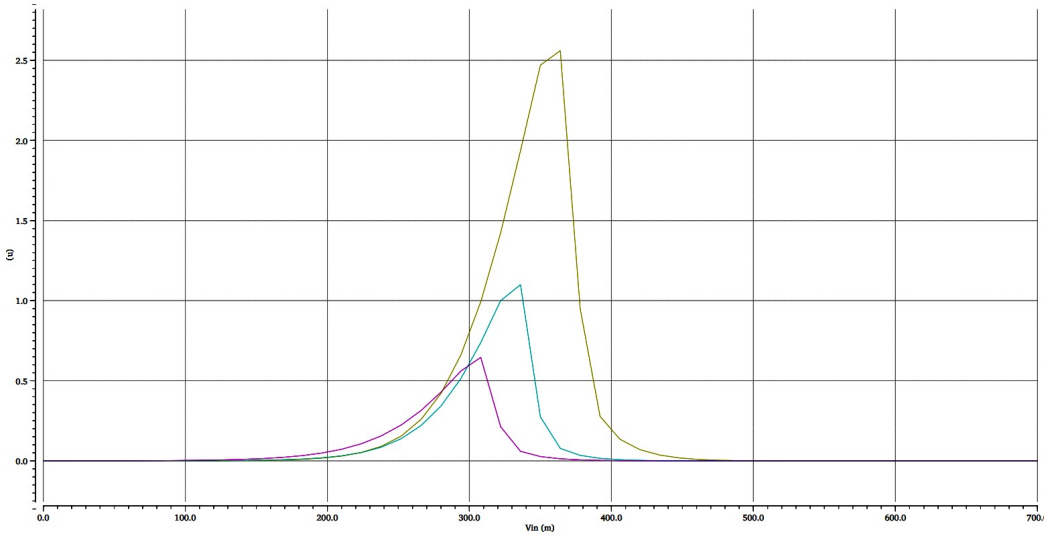

Fig. 4.14. INVx1 RVt multi-corner DC P_n.

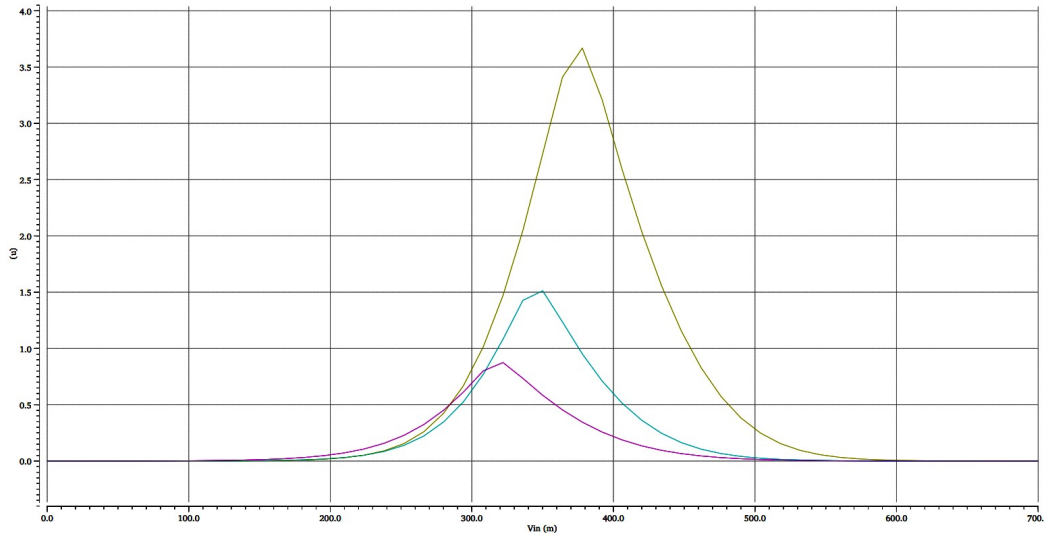

Fig. 4.15. INVx1 RVt multi-corner DC P_p.

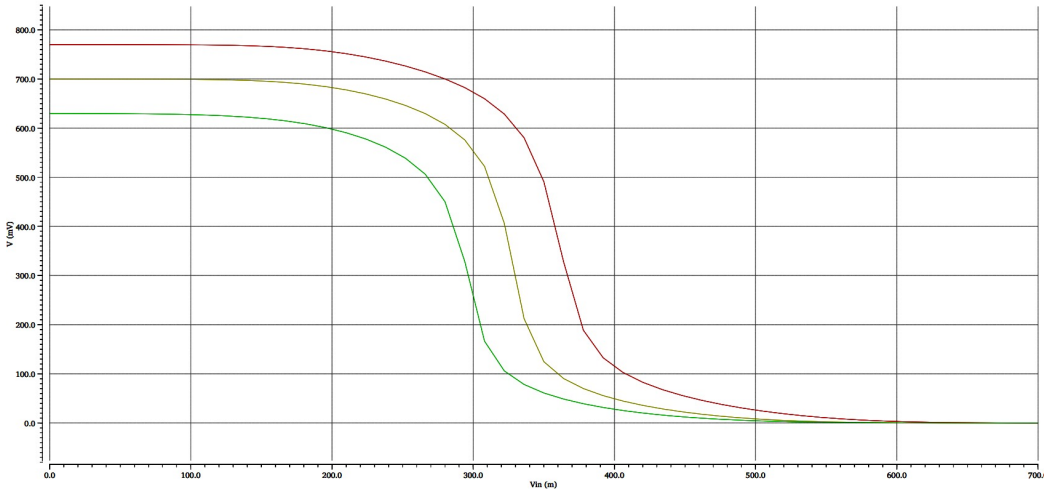

Fig. 4.16. INVx1 SLVt multi-corner VTC.

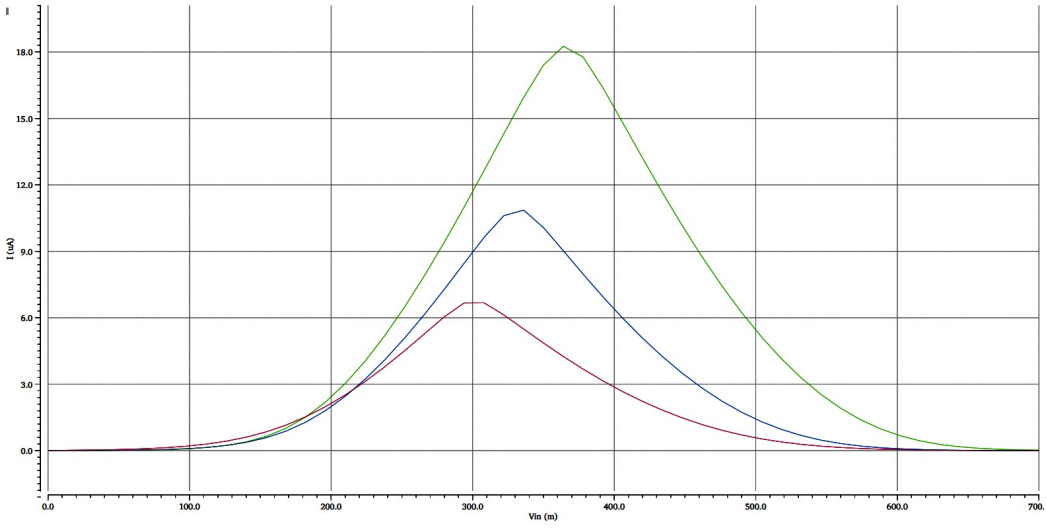

Fig. 4.17. INVx1 SLVt multi-corner I_n.

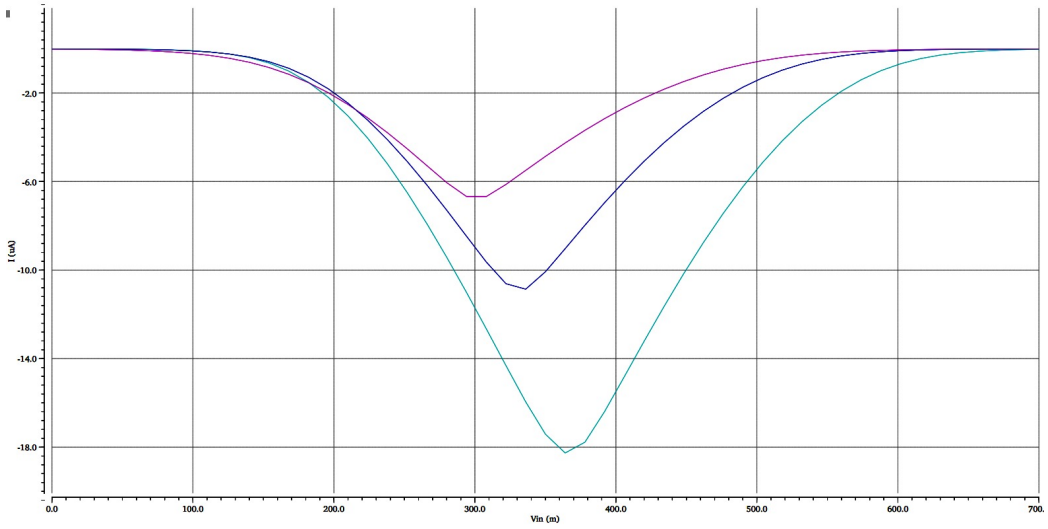

Fig. 4.18. INVx1 SLVt multi-corner I_p.

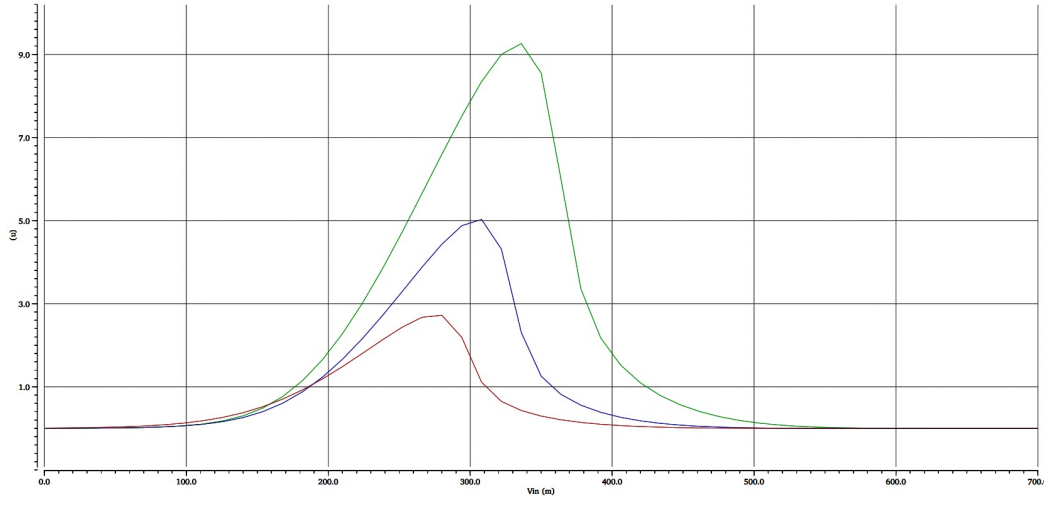

Fig. 4.19. INVx1 SLVt multi-corner DC P_n.

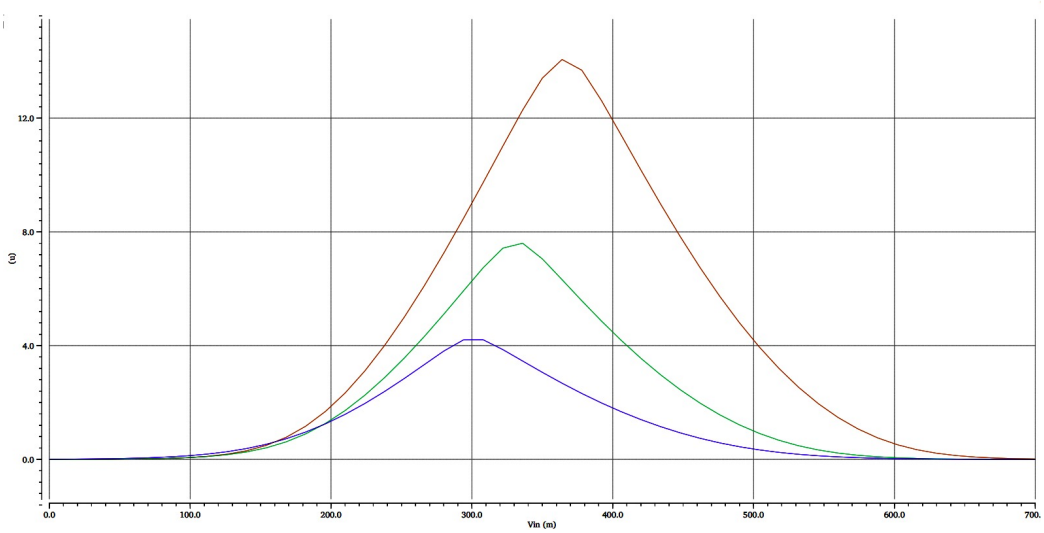

Fig. 4.20. INVx1 SLVt multi-corner DC P_p.

Table 4.1.
INVx1 LVt cell NMOS parameters

INV Lvt NMOS	V_{DD}(V)	$Temp$	V_{th} (V)	I_n (uA)	C_{gg} (aF)	P_{dc} (uW)
SS	0.63	100	255.4	3.62	55.85	1.54
TT	0.7	25	267	5.41	66.88	2.83
FF	0.77	0	272.7	10.80	82.76	5.70

Table 4.2.
INVx1 LVt cell PMOS parameters

INV Lvt PMOS	V_{DD}(V)	$Temp$	V_{th} (V)	I_p (uA)	C_{gg} (aF)	P_{dc} (uW)
SS	0.63	100	-193.2	-3.62	21.13	2.23
TT	0.7	25	-233.4	-5.41	22.57	4.11
FF	0.77	0	-247.2	-10.80	24.05	8.33

Table 4.3.
INVx1 RVt cell NMOS parameters

INV RVt NMOS	V_{DD}(V)	$Temp$	V_{th} (V)	I_n (uA)	C_{gg} (aF)	P_{dc} (uW)
SS	0.63	100	320.4	1.23	54.99	0.65
TT	0.7	25	332	2.28	65.81	1.14
FF	0.77	0	337.7	4.76	81.31	2.56

Table 4.4.
INVx1 RVt cell PMOS parameters

INV RVt PMOS	V_{DD}(V)	$Temp$	V_{th} (V)	I_p (uA)	C_{gg} (aF)	P_{dc} (uW)
SS	0.63	100	-251	-1.23	21.12	0.86
TT	0.7	25	-291.3	-2.28	22.56	1.51
FF	0.77	0	-305.4	-4.76	24	3.65

Table 4.5.
INVx1 SLVt cell NMOS parameters

INV SLVt NMOS	V_{DD}(V)	$Temp$	V_{th} (V)	I_n (uA)	C_{gg} (aF)	P_{dc} (uW)
SS	0.63	100	195	6.67	56.50	2.95
TT	0.7	25	206.6	10.86	67.66	5.0
FF	0.77	0	212.2	18.26	83.79	9.25

Table 4.6.
INVx1 SLVt cell PMOS parameters

INV SLVt PMOS	V_{DD}(V)	$Temp$	V_{th} (V)	I_p (uA)	C_{gg} (aF)	P_{dc} (uW)
SS	0.63	100	-133.2	-6.67	21.20	4.40
TT	0.7	25	-173.4	-10.86	22.63	7.50
FF	0.77	0	-187.2	-18.26	24.56	14.75

Table 4.7.
INVx1 cell TT corner NMOS parameters

INV NMOS TT	V_{DD}(V)	$Temp$	V_{th} (V)	I_n (uA)	C_{gg} (aF)	P_{dc} (uW)
SLVT	0.7	25	206.6	10.86	67.66	5.0
LVT	0.7	25	267	5.41	66.88	2.83
RVT	0.7	25	332	2.28	65.61	1.14

Table 4.8.
INVx1 cell TT corner PMOS parameters

INV PMOS TT	V_{DD}(V)	$Temp$	V_{th} (V)	I_p (uA)	C_{gg} (aF)	P_{dc} (uW)
SLVT	0.7	25	-173.4	-10.86	21.20	7.50
LVT	0.7	25	-233.4	-5.41	22.57	4.11
RVT	0.7	25	-291.3	-2.28	22.56	1.51

of input voltage to reach 50% of the output voltage. The differential equation of the delay calculation is based on the equation:

$$I = C(dV/dt) \tag{4.1}$$

The logic gates driving other logic gates in a digital system can be represented in three parts: driver, interconnect, and the load. NLDM models the drivers as a voltage source in series with a resistance. The interconnect driven by the driver can be modeled as L, T, and Pi models. The Pi models are highly accurate as compared to the other models and need fewer segments to present a big interconnect in distributed form. Delay through any wire is the multiplication of the wire's resistance R and the coupling capacitance C from the parallel wire running on the chip. The third part of the representation is the load capacitance (C_L) that counts the gate capacitance of the next stage logic. Equation 3.1 in the previous chapter of this dissertation explains all about the gate capacitance of any transistor. The schematic in Figure 4.30 depicts the test-bench created on the Cadence Virtuoso. In the next figure, the analysis results are shown. An inverter driving no capacitance at the output suffers the problem of the bootstrapping caused by the gate to drain capacitance of the cell and can be seen as the overshoot and undershoot at every logic change. The inverter cell driving a variable capacitance (for 0.2 to 0.1fF) is analyzed for the propagation delay at multiple corners for all available threshold voltage transistor variants. The comparisons are shown in Table 4.9, 4.10 and 4.11.

Table 4.9.
INVx1 LVt cell multi-corner variable capacitance t_{pd} (ps)

INV LVt	V_{DD}(V)	$Temp$	$C_L = 0.2$(fF)	$C_L = 0.5$(fF)	$C_L = 0.7$(fF)	$C_L = 1$(fF)
SS	0.7	100	4.25	7.00	8.74	11.37
TT	0.7	25	4.11	6.72	8.38	10.84
FF	0.77	0	3.96	6.39	7.91	10.18

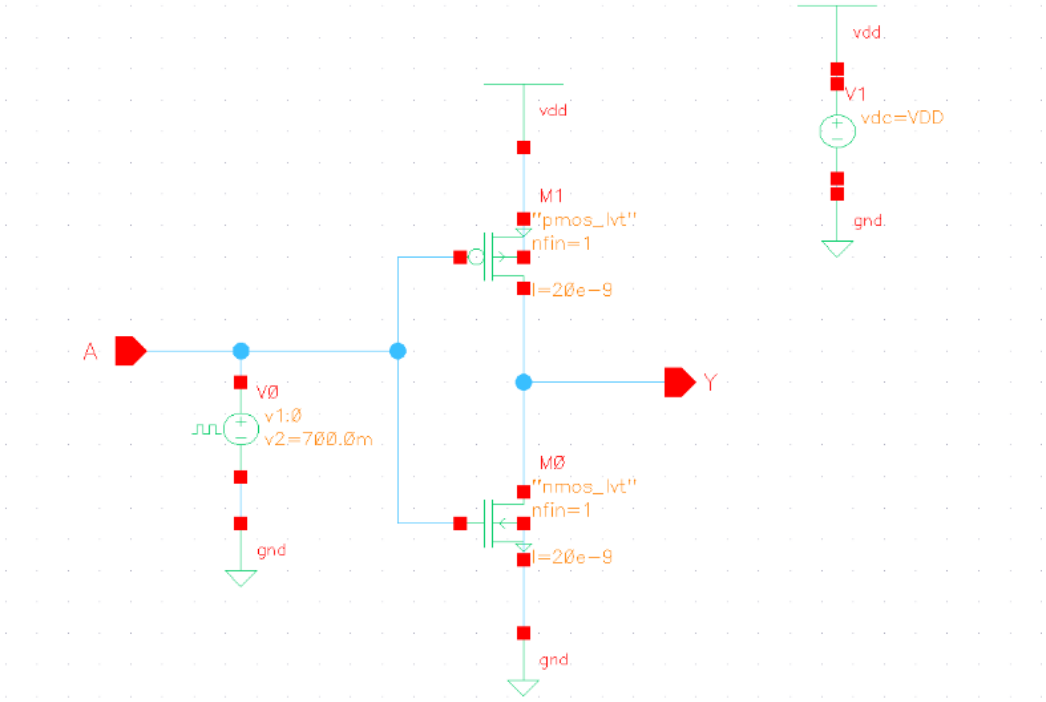

Fig. 4.21. INVx1 LVt TT transient analysis set-up without load capacitance.

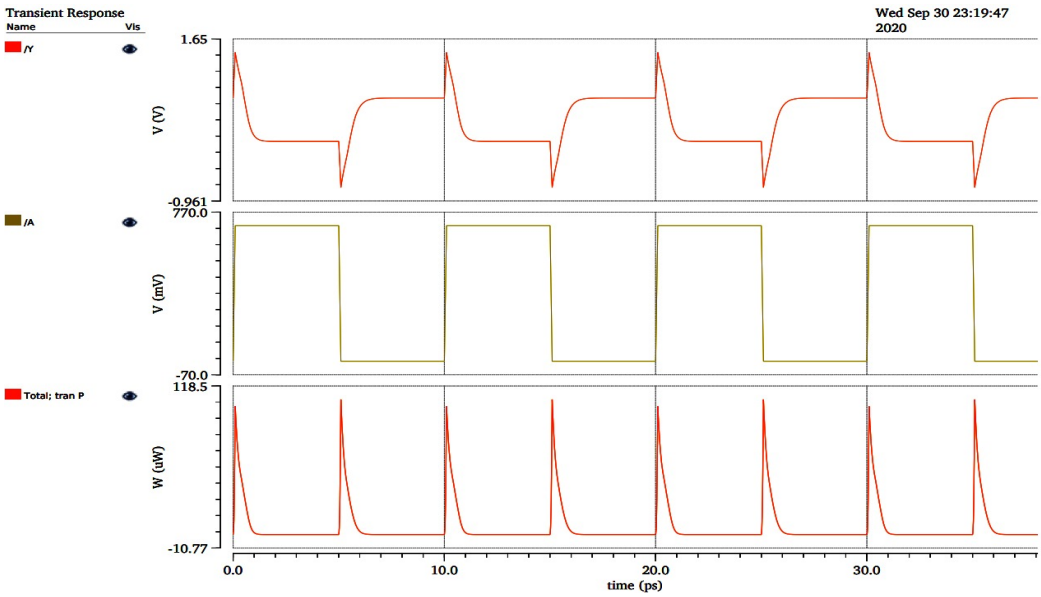

Fig. 4.22. INVx1 LVt TT corner transient waveform.

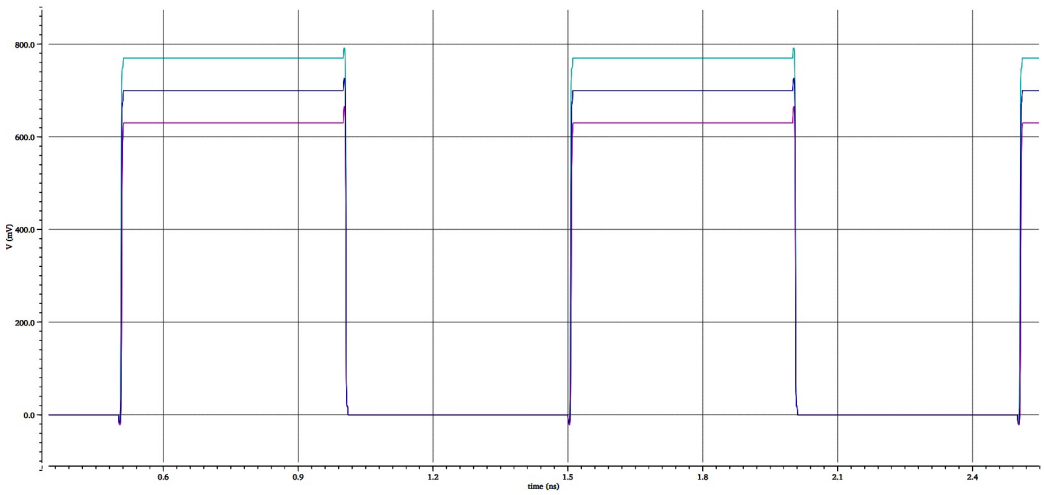

Fig. 4.23. INVx1 LVt multi-corner transient output.

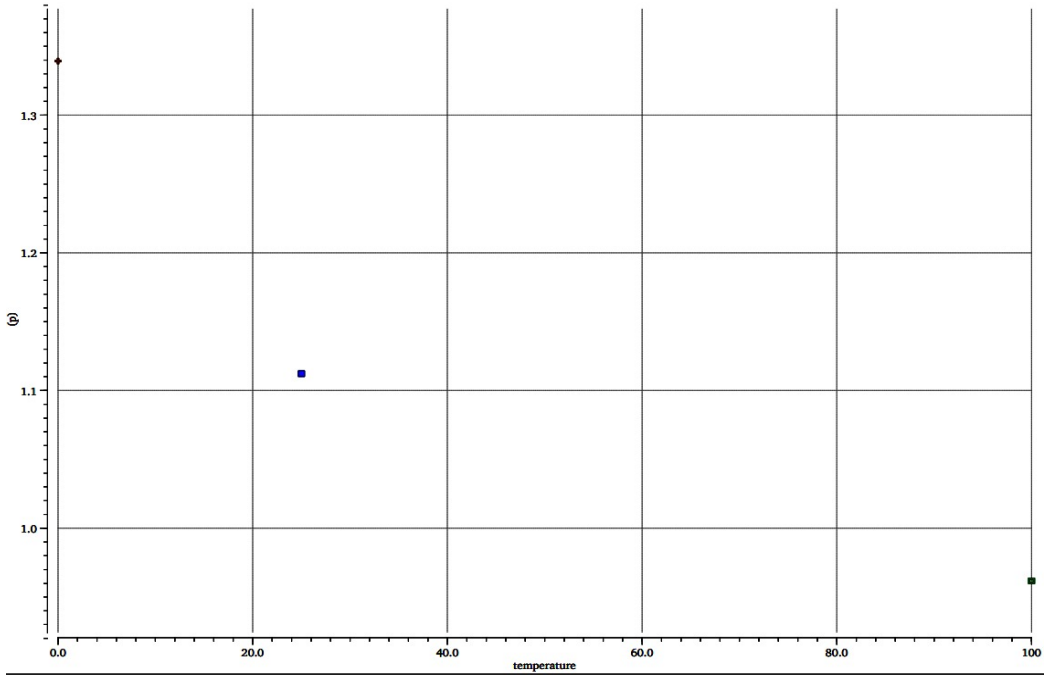

Fig. 4.24. INVx1 LVt multi-corner propagation delay.

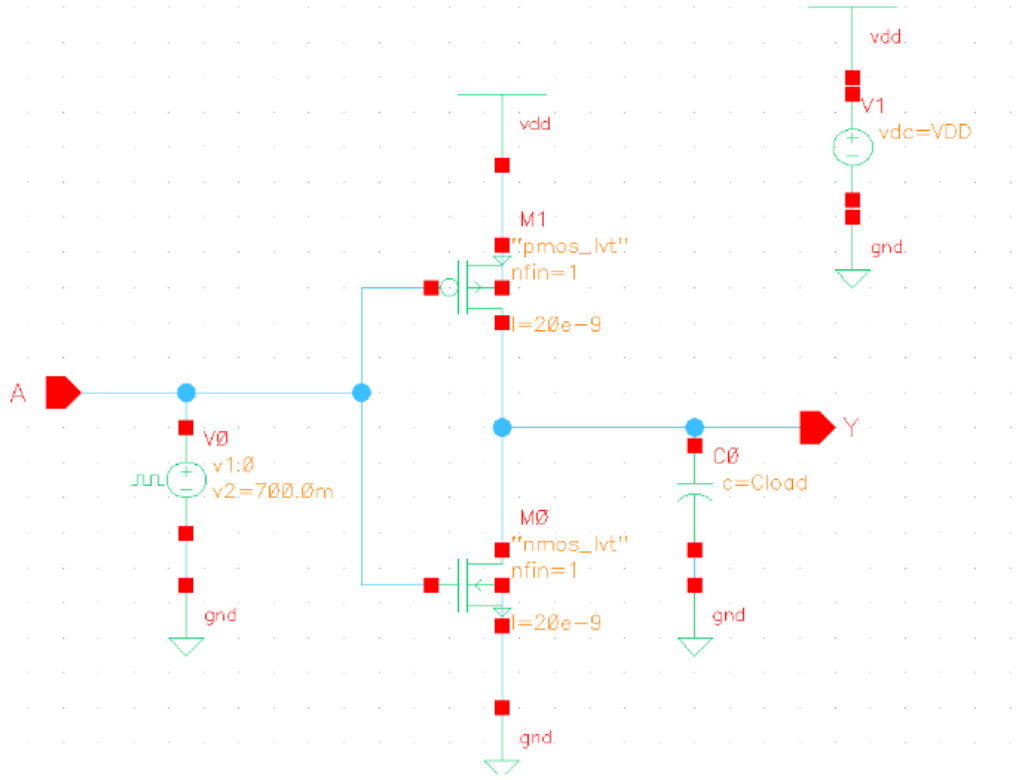

Fig. 4.25. INVx1 LVt multi-corner variable capacitance set-up.

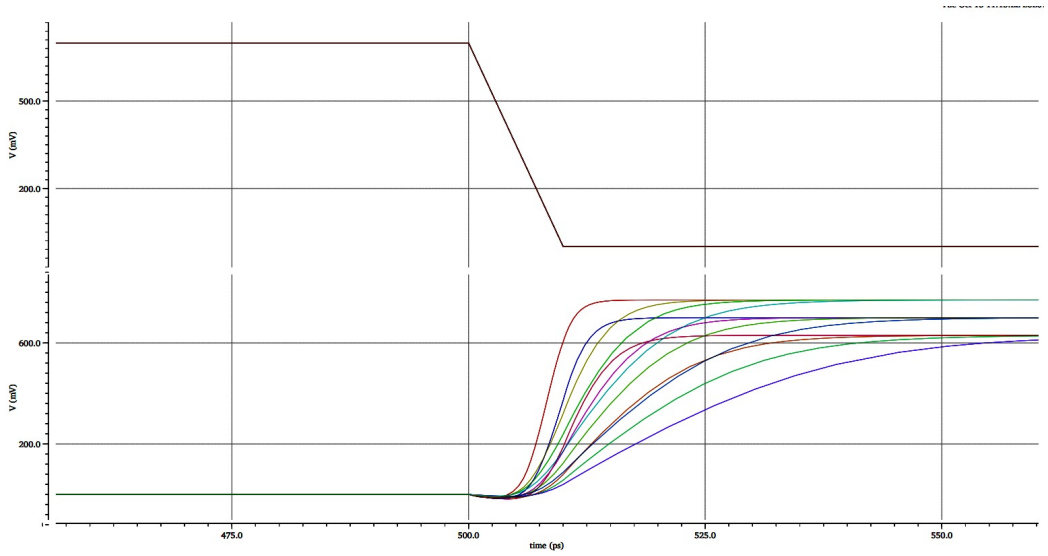

Fig. 4.26. INVx1 LVt multi-corner variable capacitance transient analysis.

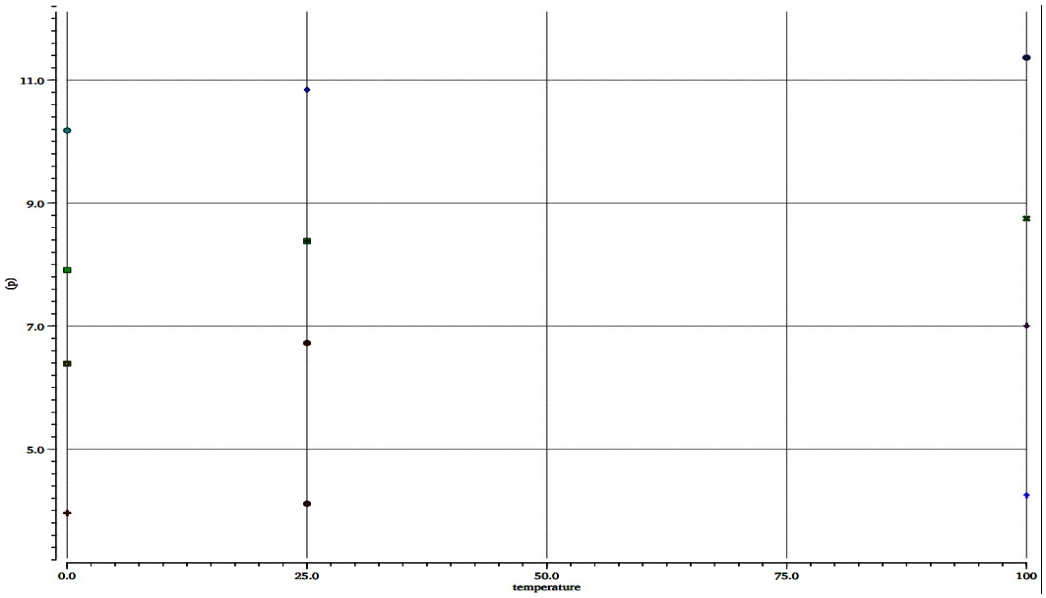

Fig. 4.27. INVx1 LVt multi-corner variable capacitance propagation delay.

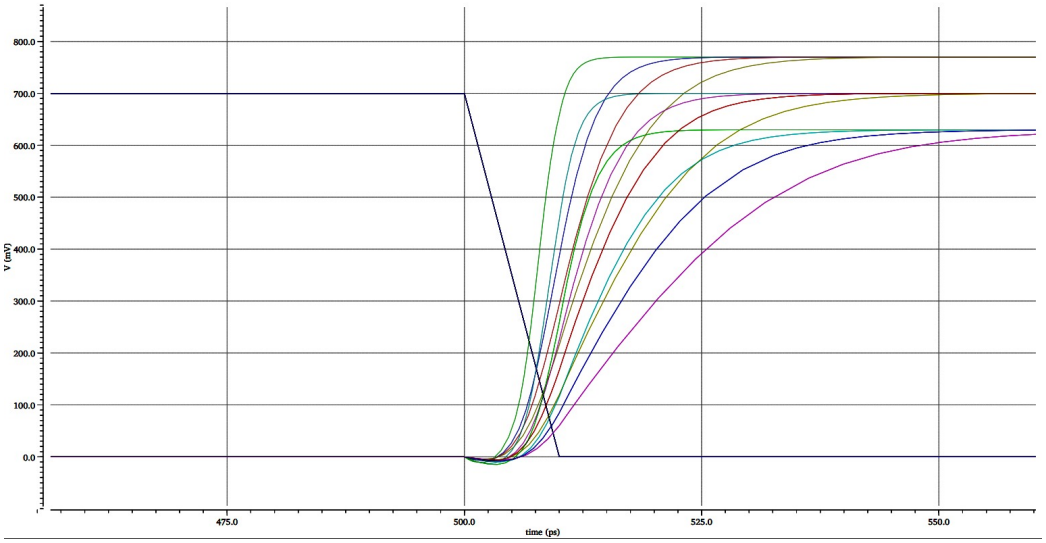

Fig. 4.28. INVx1 SLVt multi-corner variable capacitance transient analysis.

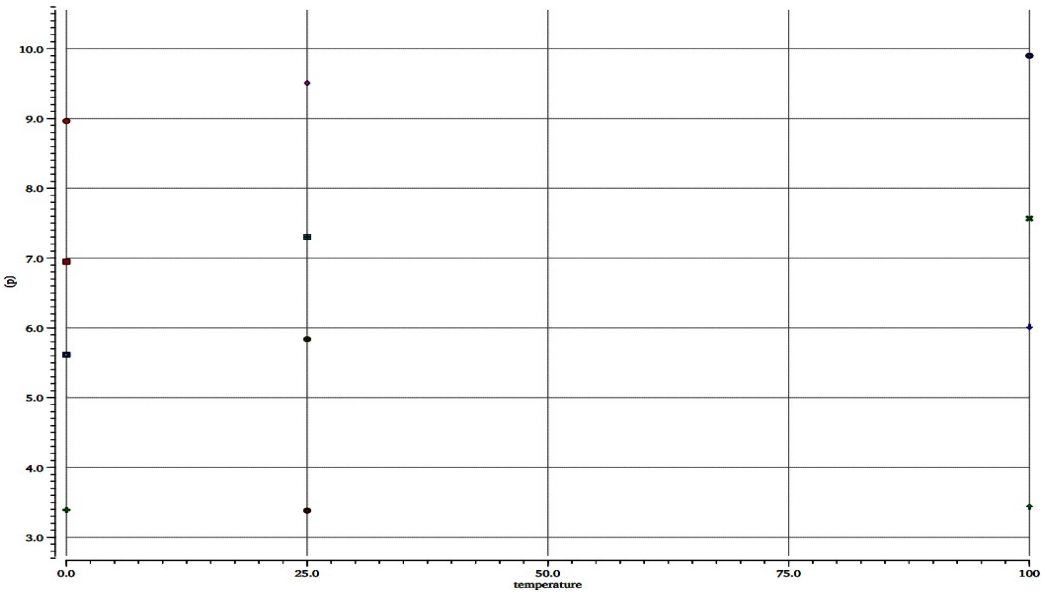

Fig. 4.29. INVx1 SLVt multi-corner variable capacitance propagation delay.

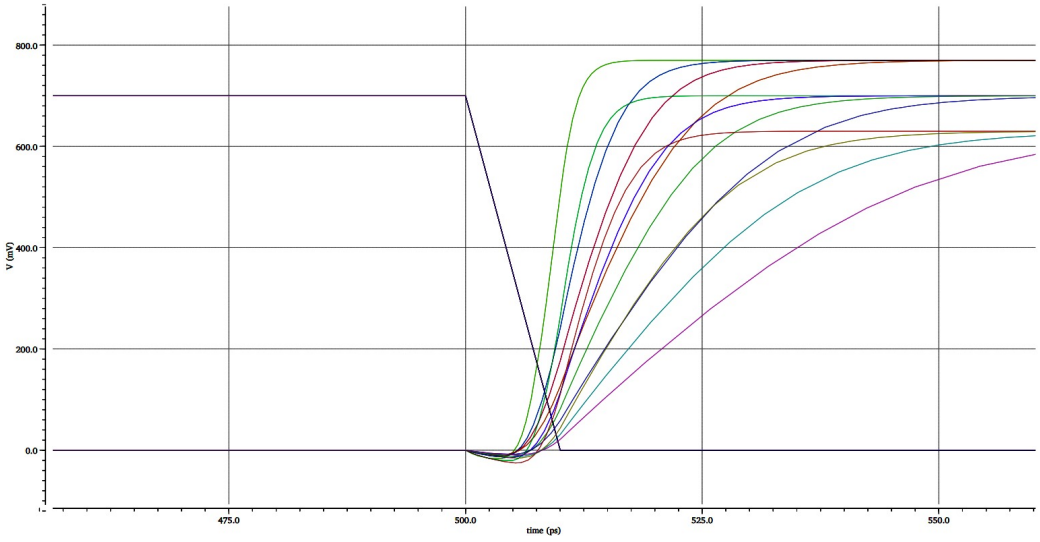

Fig. 4.30. INVx1 RVt multi-corner variable capacitance transient analysis.

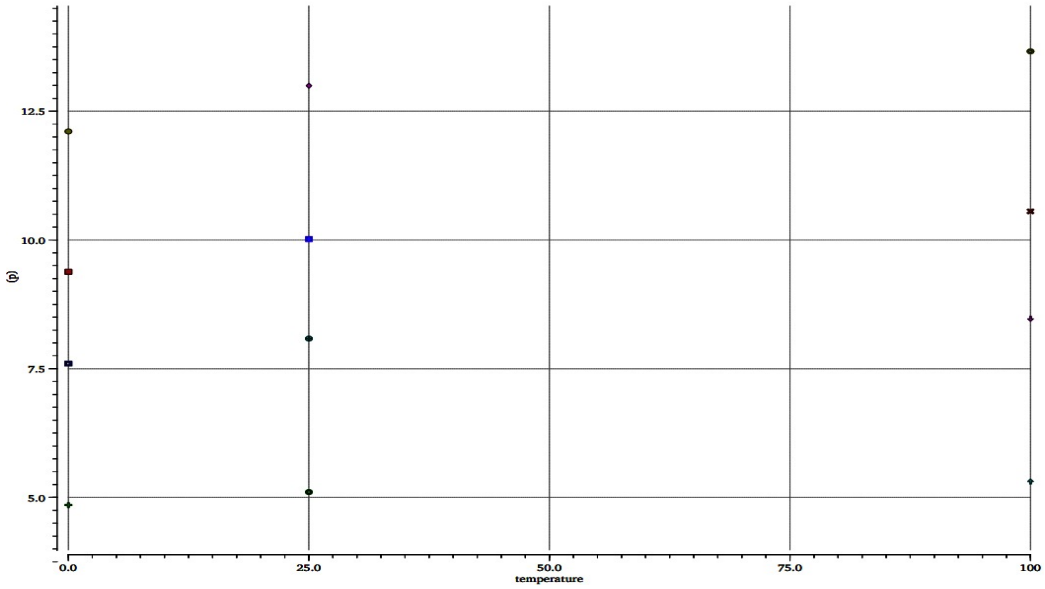

Fig. 4.31. INVx1 RVt multi-corner variable capacitance propagation delay.

Table 4.10.
INVx1 SLVt cell multi-corner variable capacitance t_{pd} (ps).

INV SLVt	V_{DD}(V)	$Temp$	$C_L = 0.2$(fF)	$C_L = 0.5$(fF)	$C_L = 0.7$(fF)	$C_L = 1$(fF)
SS	0.7	100	3.43	6.01	7.56	9.90
TT	0.7	25	3.83	5.83	7.30	9.50
FF	0.77	0	3.39	5.61	6.94	8.96

Table 4.11.
INVx1 RVt cell multi-corner variable capacitance t_{pd} (ps)

INV RVt	V_{DD}(V)	$Temp$	$C_L = 0.2$(fF)	$C_L = 0.5$(fF)	$C_L = 0.7$(fF)	$C_L = 1$(fF)
SS	0.7	100	5.31	8.47	10.56	13.66
TT	0.7	25	5.10	8.08	10.02	13.00
FF	0.77	0	4.85	7.60	9.38	12.11

4.3 Robust Clock Repeaters

The interconnects play important roles in modern systems and are key to the performance. A wire connecting two transistors is consisted of metal and has some specific width. Each wire geometry has resistance in it that is given by the following equation:

$$R = \rho L/A \tag{4.2}$$

Equation 4.2 shows the importance of the length and the cross-sectional area in the resistance estimation. In digital design, every metal used for the routing has some specific width and hence resistance. Routing of wires in the physical design implementation exhibit capacitance as well. The capacitance term is contributed by some individual components: fringing field and parallel plate capacitances. Overall capacitances are given by the following equation:

$$C = \epsilon_o A/d \tag{4.3}$$

Modern designs with sub-nanometer processes carefully consider the interconnect length and width while driving some load capacitance [36]. The delay through the wire, flight time (RC), has the value in the order of a cell delay. Hence to drive the cell sitting on the far end, the repeaters are required. In physical design, the clock tree synthesis is one of the applications that neutralizes the delay through the long interconnect connecting the clock pins of sequential elements using clock repeaters. There are following well-known methodologies for clock implementation in a design [37].

- H Clock Tree
- Clock Three Mesh
- Binary Clock Tree

The first two methods are used in a block-level design and ensure that the clock skew requirement is met with the desirable performance [38]. System on Chip (SoC) clocks are implemented using global clock distribution methodology [39]. This method uses a binary clock network to drop the clock until physical blocks inside the SoCs. Routing resources and latencies are the main targets to achieve during implement ion. Each of the clock implementation methods uses the clock repeaters to regenerate the distorted clock signal. Hence, the inverter cells presented in the previous two sections of this chapter propose a robust clock repeater for the high-performance designs. Before investigating the reason for performance and robustness, it is important to understand a CMOS inverter capacitances and sizing. Figure 4.32 depicts a CMOS inverter with width sizing to achieve equal rise and fall transitions. The obvious reason for the twice width of the PMOS is its lower mobility.

The FinFET technology does not require width matching and provides symmetric rise and fall transitions with an equal number of fins [11]. This assists in the performance of clock repeaters picked for reducing the delay of a long wire. To test the switching speed of INV as clock repeaters, a test-bench was created to examine the FO6 delay. Figure 4.36 shows the schematic created on Cadence Virtuoso. The third inverter with drive strength 36 is under analysis for the delay calculation.

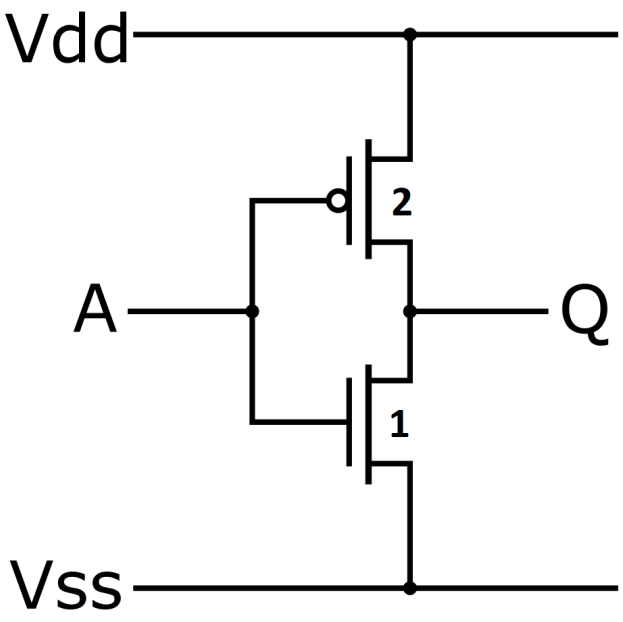

Fig. 4.32. CMOS inverter sizing.

Figure 4.34 and 4.35 shows the difference input pin capacitance of a CMOS driving FO4 and FinFET driving FO6 inverters. The load capacitance is equal to the CMOS inverter seeing at its output. Hence, a FinFET inverter drives the same load capacitance for FO6 delay to achieve the smallest possible delay for minimum path effort. The results are compared in table 4.12 for LVt transistors on the TT corner.

Table 4.12.
INVx36 LVt cell TT corner FO6 t_{pd} (ps)

INV LVt	V_{DD}(V)	$Temp$	$t_{pd}FO6$(ps)
SS	0.63	100	13.40
TT	0.7	25	11.01
FF	0.77	0	9.76

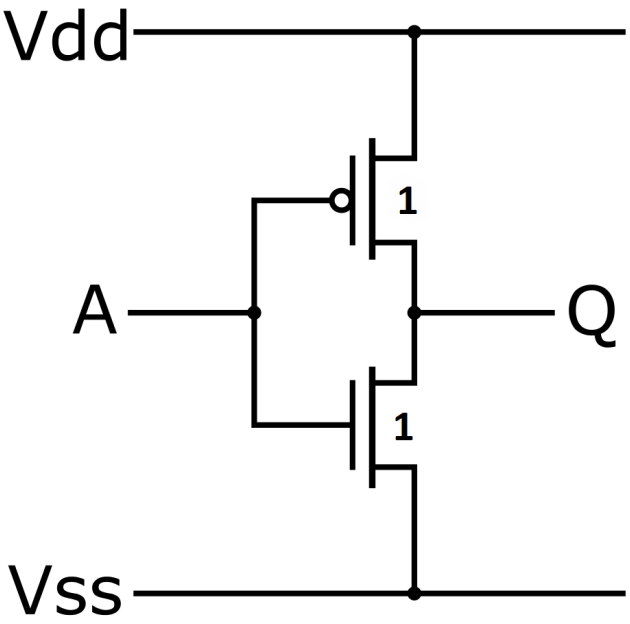

Fig. 4.33. FinFET inverter sizing.

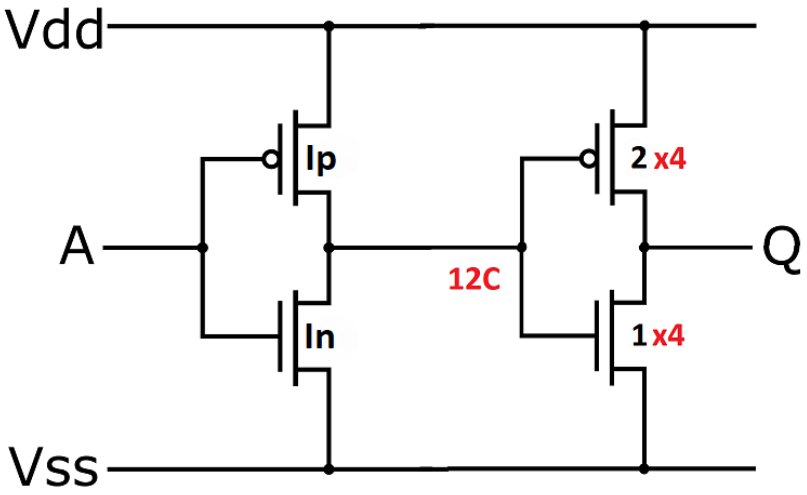

Fig. 4.34. CMOS driving FO4.

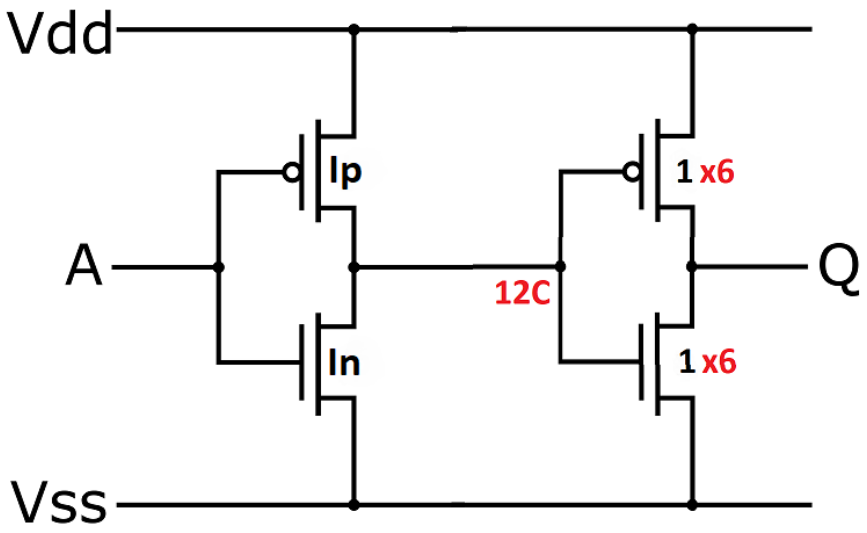

Fig. 4.35. FinFET driving FO6.

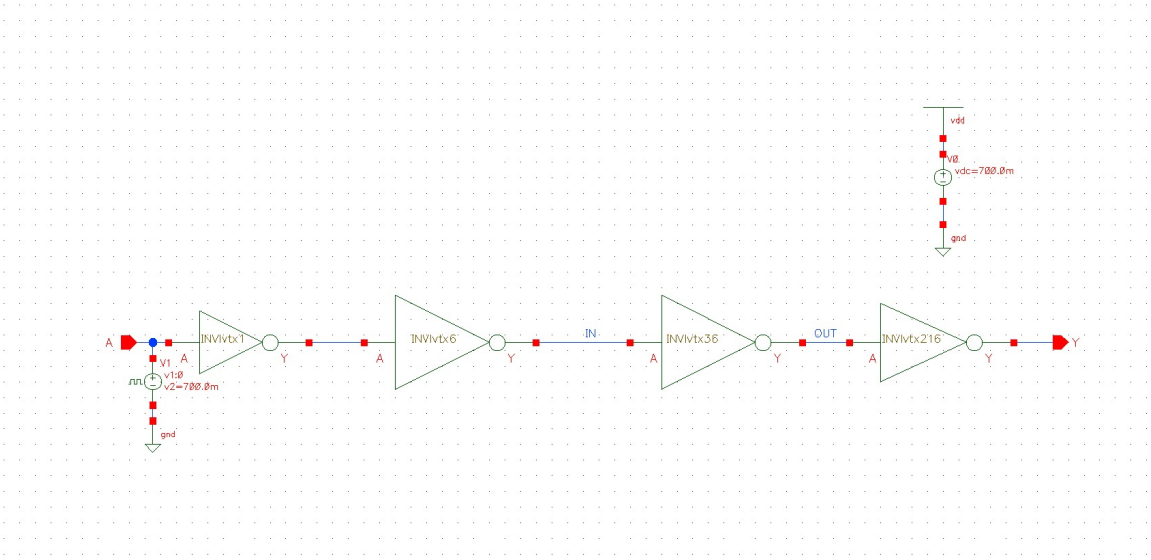

Fig. 4.36. FinFET driving FO6 schematics.

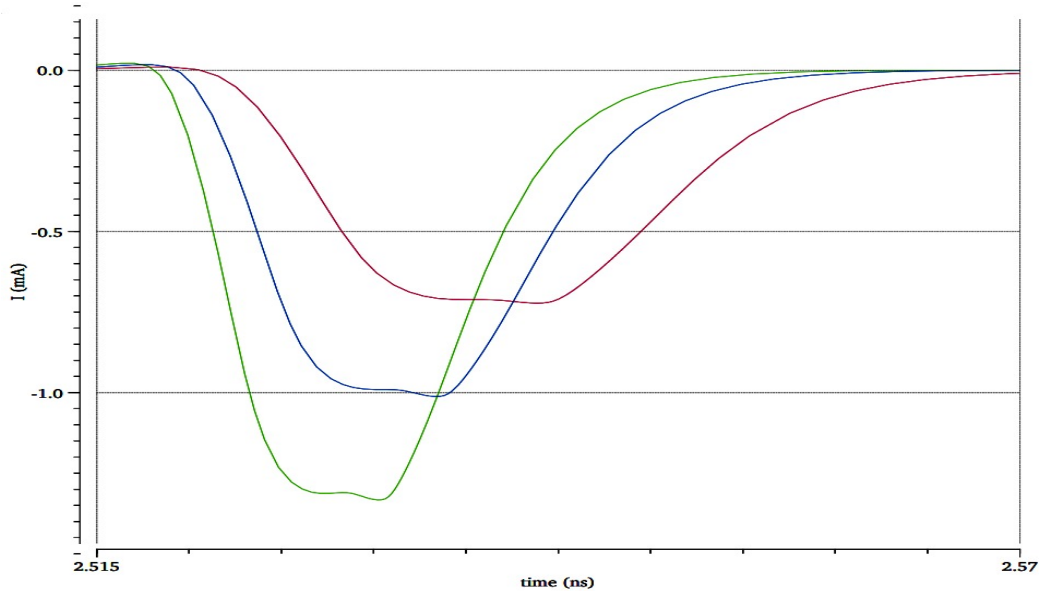

Fig. 4.37. FO6 PMOS current.

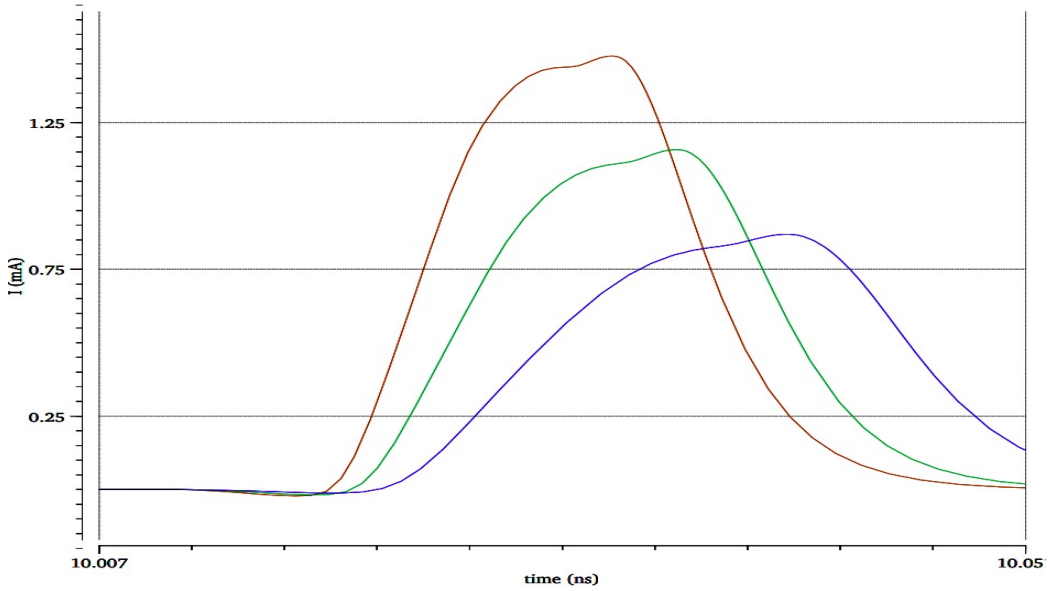

Fig. 4.38. FO6 NMOS current.

5. MEMORY DESIGN

Semiconductor memories are capable of storing a vast amount of digital information. Memory components are ubiquitous in modern integrated circuits. Modern microprocessor's caches are one such example of its extensive presence in ICs. Caches are categorized under on-chip memory that shares the same die with microprocessor cores. The area efficiency of the memory array is one of the key design criteria that determines the storage capacity. Speed is another key design feature of the memory and signifies the time required to store or retrieve information. Finally, static and dynamic power consumption is considered as another significant factor in memory design. Random Access Memories is the memory arrays that are accessed using the address and they are divided into two parts: Read Only Memory (ROM) or Non-volatile Memory and Volatile Memory [29]. There are two different kinds of volatile RAMs based on the operation type of individual data storage cells.

- Static RAM
- Dynamic RAM

The static RAM cell can retain the data indefinitely as long as the power supply is provided. However, the dynamic SRAM cell needs to be refreshed periodically so that its contents do not leak. Both the SRAM store data differently. Static SRAM cell stores the data in feedback look to maintain its state whereas a dynamic SRAM cell stores data as a charge on a capacitor [29]. The feedback loop in a static SRAM cell is consists of a simple latch formed using inverter cells and stores 1-bit of operation. This retention capability can also be achieved by a flip-flop but flop implementation takes more area as compared to SRAMs. The standard 6T SRAM cell provides a denser layout and better performance than a normal flip-flop cell. It achieves compactness at the expense of complex circuitry involved in designing. For these aforementioned

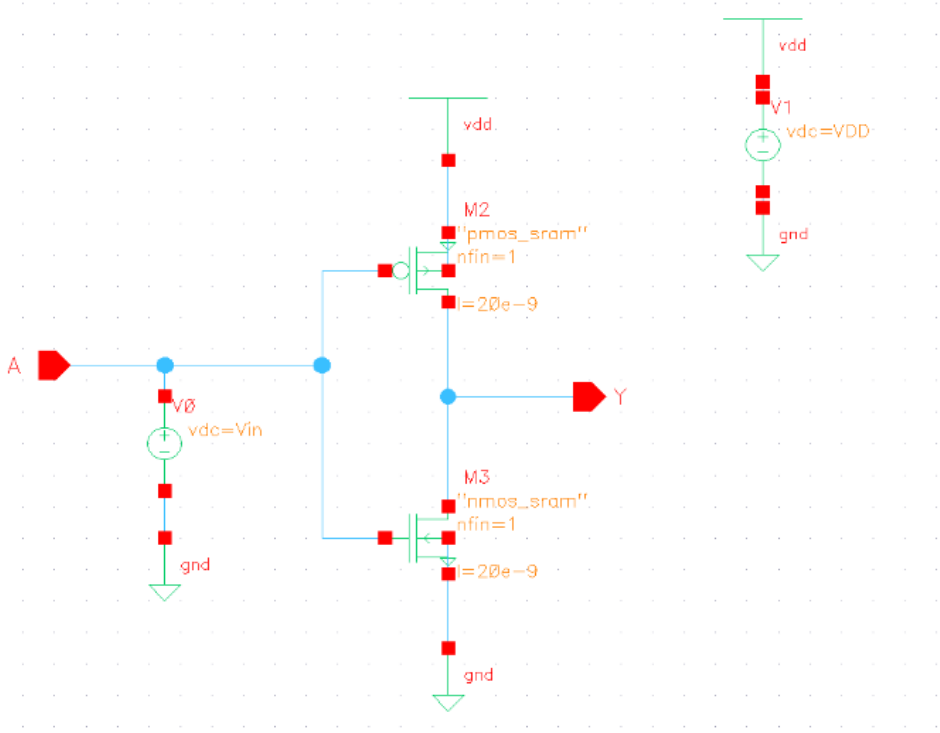

Fig. 5.1. INVx1 SRAM Vt schematic.

reasons, static SRAMs are used in myriad applications from microprocessor caches to register files. In this dissertation, the focus is to present a robust six-transistor (6T) static RAM cell and characterize it on multiple corners.

5.1 ASAP7 SRAM Vt Transistors

The 7nm FinFET library comes with "sram" transistor flavor that is high threshold voltage transistors characterized by low leakage power and high efficiency [18].

5.2 6T SRAM Cell

The 6T SRAM cell retains the data in weak cross-coupled inverters forming a latch with two NMOS transistors providing read and write facility to the cell. The

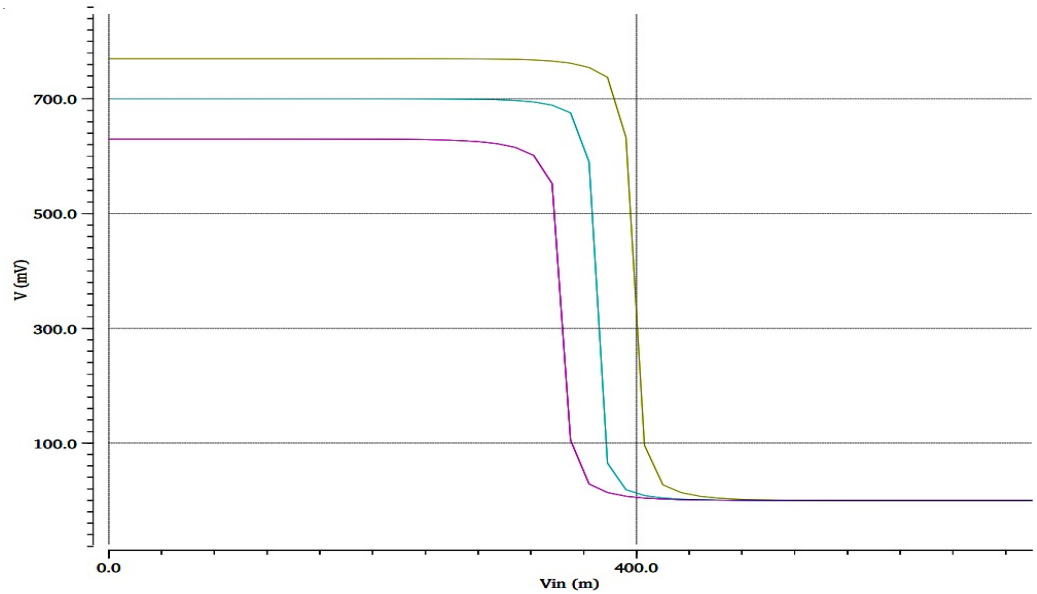

Fig. 5.2. VTC INXx1 SRAM Vt cell.

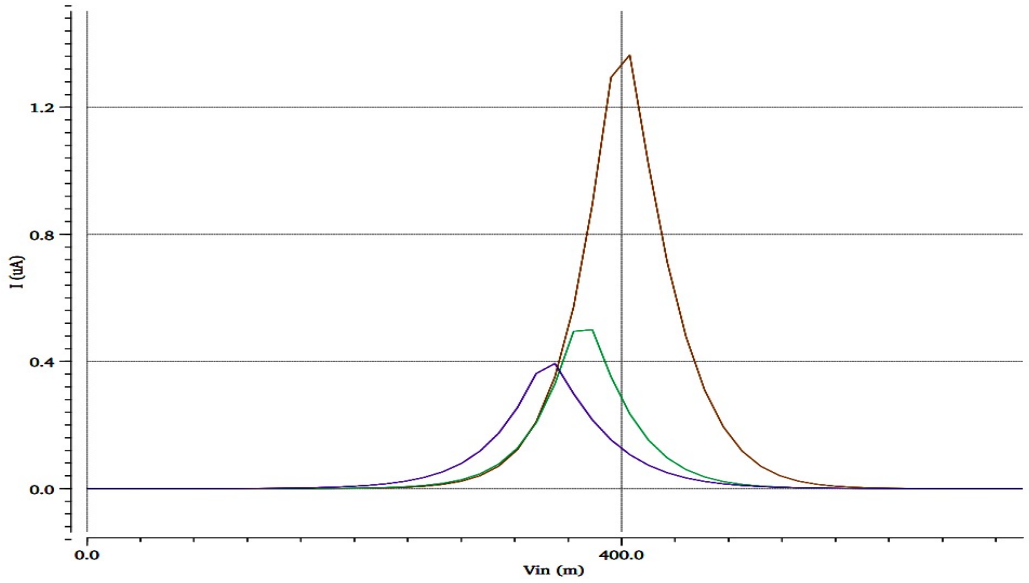

Fig. 5.3. INXx1 SRAM Vt I_n.

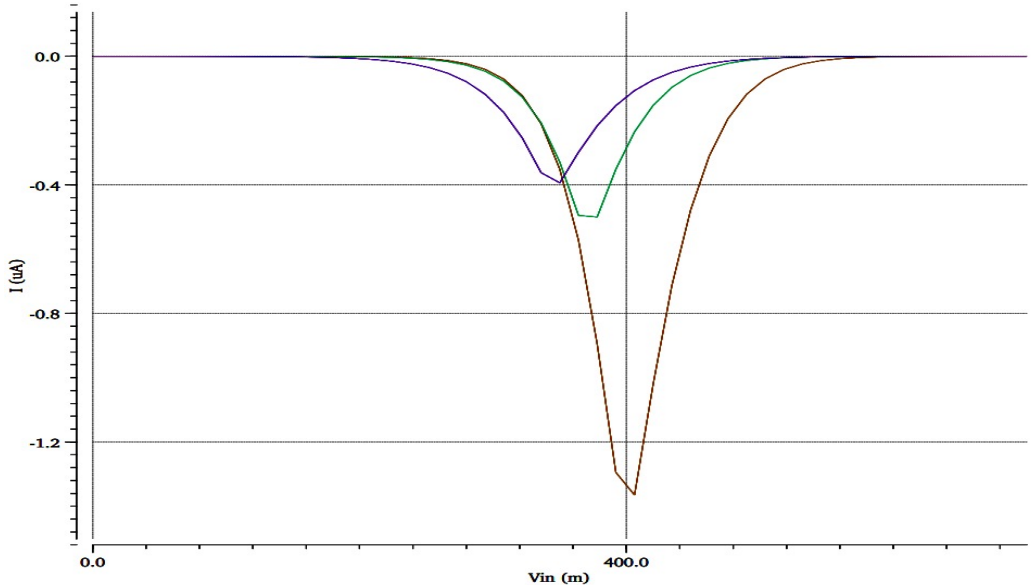

Fig. 5.4. INXx1 SRAM Vt I_p.

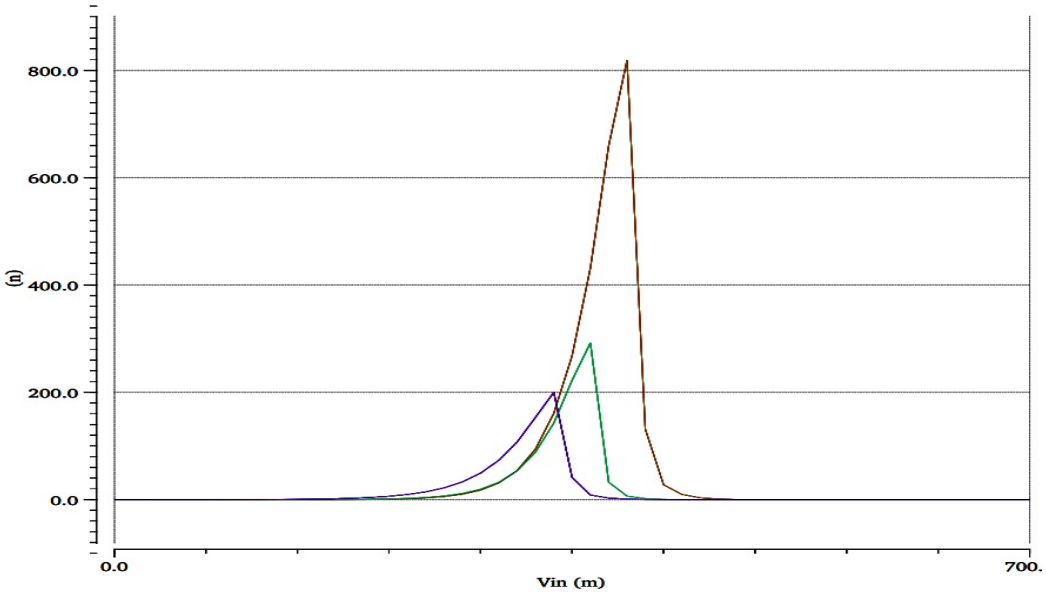

Fig. 5.5. INXx1 SRAM Vt P_n.

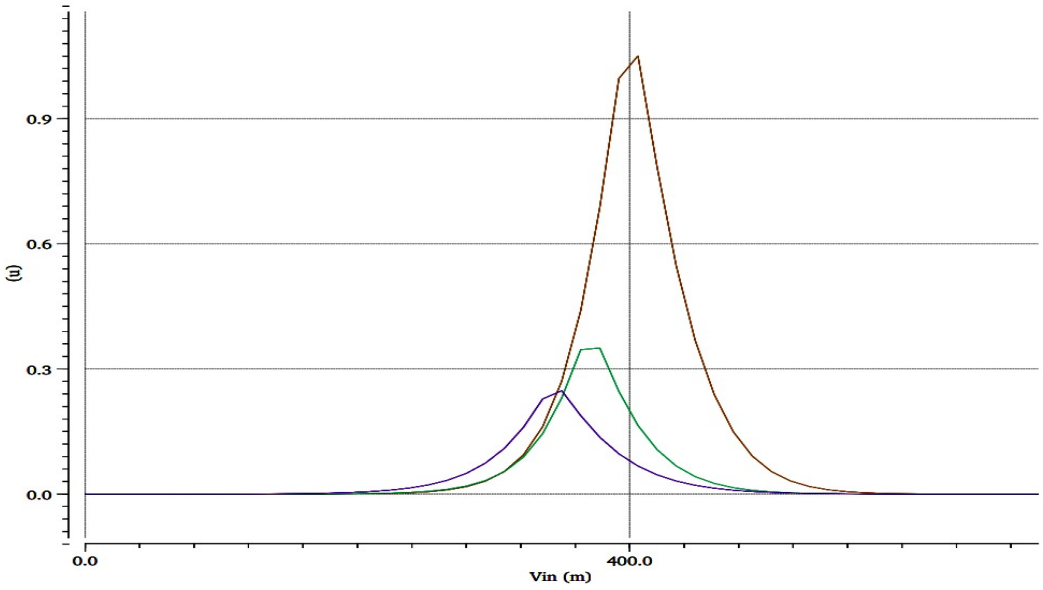

Fig. 5.6. INXx1 SRAM Vt P_p.

Table 5.1.
INVx1 SRAM cell NMOS parameters

INV SRAM NMOS	V_{DD}(V)	$Temp$	V_{th} (mV)	I_n (uA)	C_{gg} (aF)	P_{dc} (uW)
SS	0.63	100	395.6	0.38	19.14	0.20
TT	0.7	25	406.2	0.50	20.45	0.29
FF	0.77	0	410.7	1.36	21.75	0.81

Table 5.2.
INVx1 SRAM cell PMOS parameters.

INV SRAM PMOS	V_{DD}(mV)	$Temp$	V_{th} (V)	I_n (uA)	C_{gg} (aF)	P_{dc} (uW)
SS	0.63	100	-294.1	-0.38	52.40	0.24
TT	0.7	25	-339.1	-0.50	63.70	0.35
FF	0.77	0	-358.8	-1.36	80.38	1.05

positive feedback in the latch corrects the stored value from the disturbances caused by the noise or leakage. The new data is written by the bit and bit_bar lines. Figure 5.7 depicts a 6T-SRAM cell with its components Word Line (WL), Bit Line (BL), Bit Bar Line (BB), Inverters, and NMOS Access transistors. When the new data is written, it overpowers the stored information inside the cross-coupled inverters. The reading operation is achieved by charging the bit line voltage up to VDD and then measuring the difference between the BL and BB lines. However, there are two requirements that dictate the operations are [40]:

- The read operation should not destroy the stored information in the SRAM.
- The cell should allow modification during the data write operation.

The aforementioned requirements put the strict sizing ratio among inverter's pullup and pulldown transistors and access transistors. For FinFET transistors, the sizing ratio is in terms of the number of fins. The design presented in this thesis possesses the number of fins ratio Pullup:Access:Pulldown to be 1:2:3. The schematic

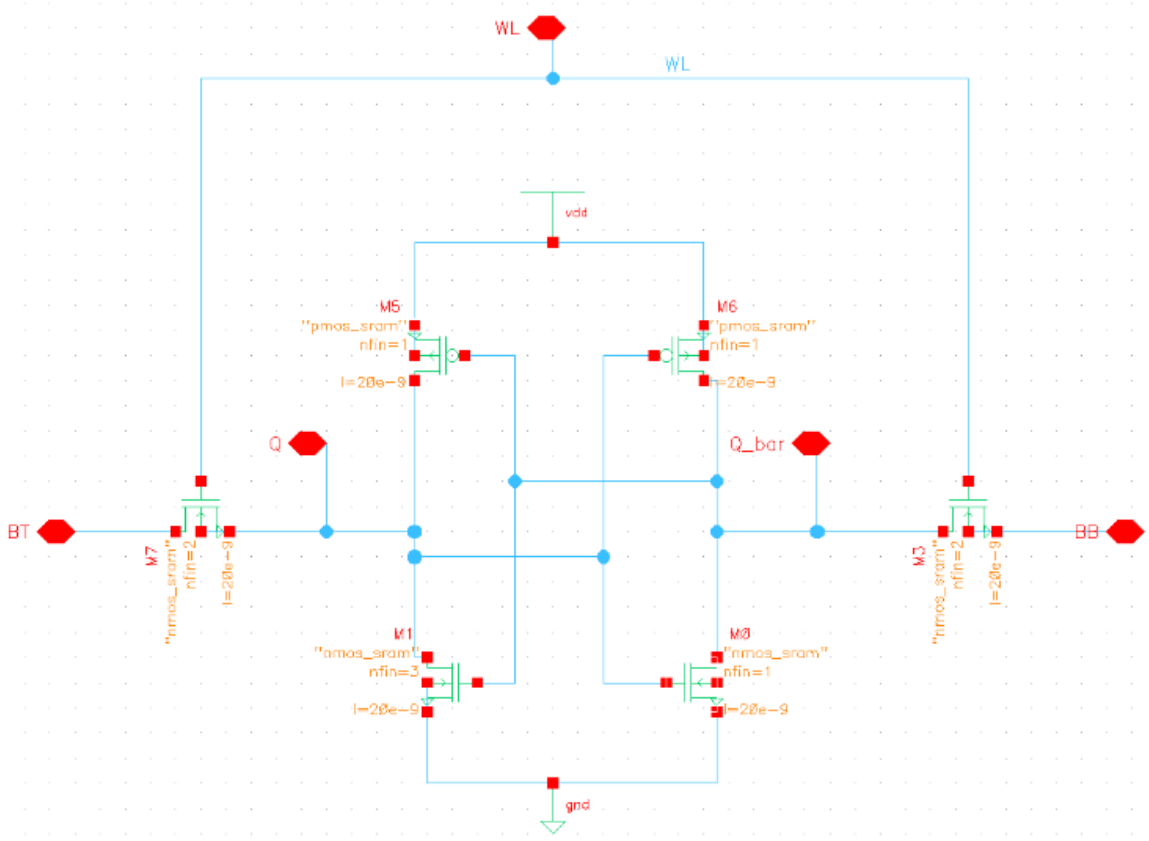

Fig. 5.7. 6T SRAM bit cell.

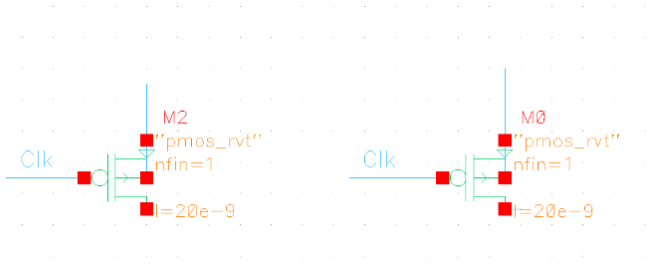

Fig. 5.8. Pre-charge transistors.

was designed on Cadence Virtuoso. The body of each transistor is grounded. All the PMOS sources are connected to VDD and NMOS sources are connected to GND. Access transistors are driven by the word line connected to the gate of the transistors whereas other terminals of access transistors are connected to Bit lines and the outputs of the cross-coupled inverters. Further sections explain the other circuitries needed to create a test bench for Read and Write operation.

5.2.1 Clocks

The SRAM operations write, read and hold require two phase clock ϕ_1 and ϕ_2 for the synchronization, and these can be generated by clock clk and its complement clkb.

5.2.2 Column Circuitry

The column circuitry consists of the bitline pre-charge circuitry, the write driver, the column multiplexers, and the bit-line sensing circuitry. Before beginning, the read or write operation the bit lines are pre-charged using pre-charge circuitry to avoid failures. Charging bit lines provides voltage to the access transistor's terminal connected to it and that begins the read/write operation. The pre-charge circuitry consists of two PMOSs FinFET transistors and is connected to the power to charge the bitline capacitances. The figure shows the pre-charge circuitry used in the analysis.

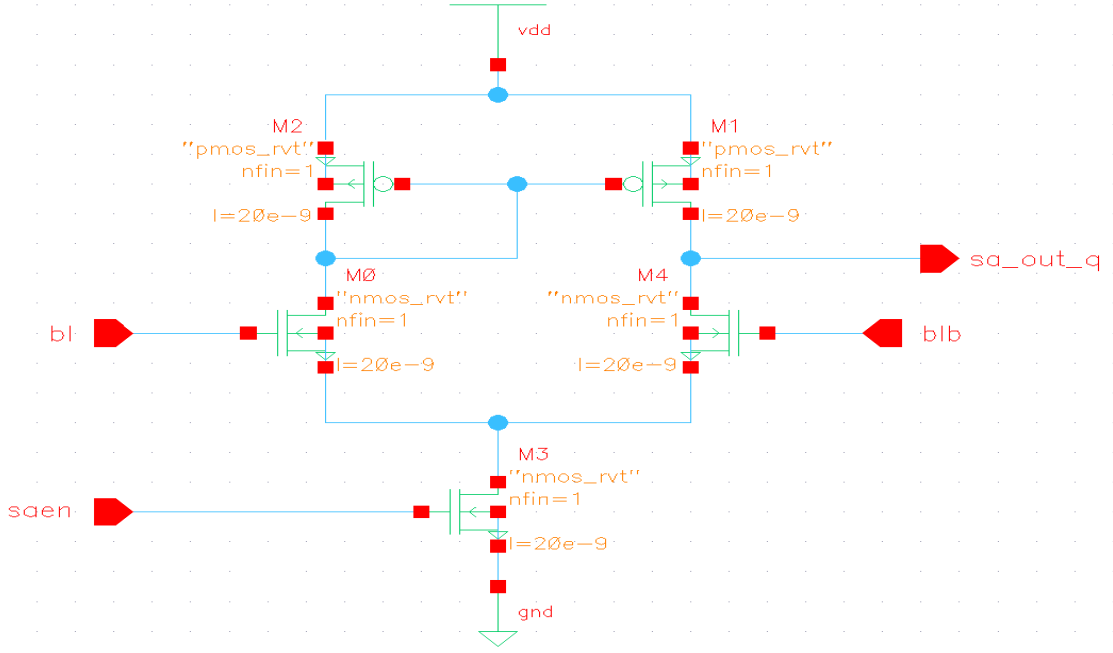

Fig. 5.9. Differential amplifier design.

Another part of the column circuitry is column multiplexers. They are required to extract the bits from each row of the SRAM array. To read bits associated with each column are considered as the inputs to the multiplexer. The select line of the multiplexer chooses the data from multiple column addresses. Generally, muxes can be implemented using the tri-state inverter and the transmission gates. The sensing circuitry is attached to the bit lines to capture the drop in either of the line and flag the output depending upon the voltages on the bit and bitbar lines. The bitline capacitance is the sum of the long wire capacitance and the access transistor capacitance on the same column address. This big capacitance is an issue in large SRAM arrays during the read operation due to the large time required to discharge this capacitance to zero. To avoid this slow discharge issue, a sense amplifier is added to column sensing circuitry. Figure 5.9 depicts the FinFET based differential amplifier circuit.

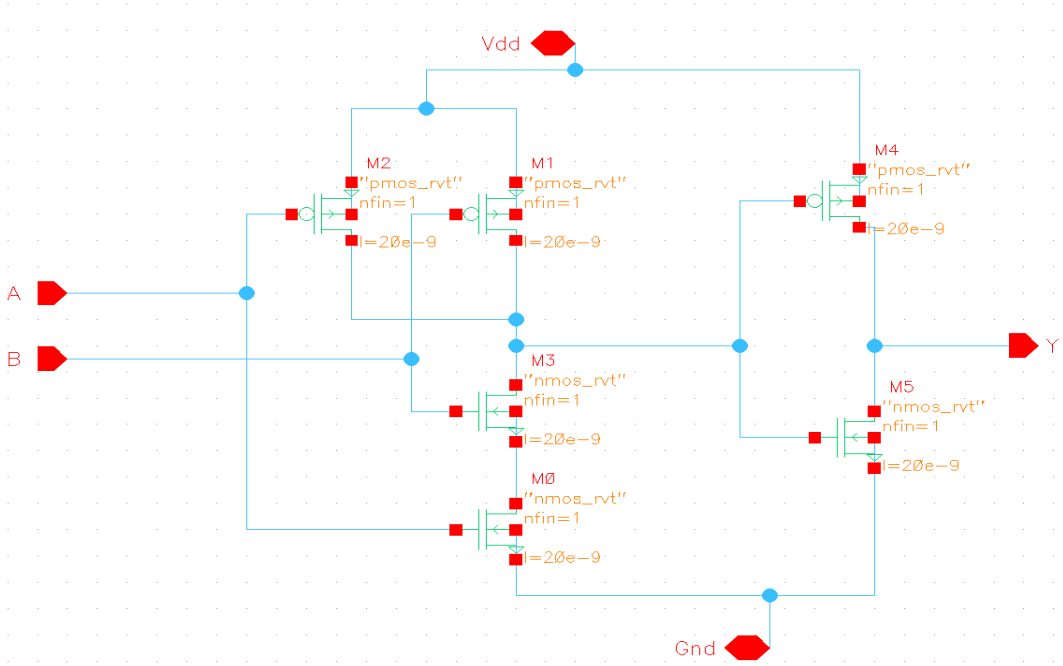

Fig. 5.10. AND gate design.

5.2.3 Row Circuitry

The row circuitry is designed using two main components: the row address decoder and the word line drivers. The AND gates are used to assert the word line and available in both true and complement versions. Figure 5.10 shows the schematic of AND gate used to design the address decoder for the design tested in this thesis. The addresses for some specific cell is ANDed with the clk to raise the word line of that SRAM cell. During the read operation, the clk and read enable (RD_En) are raised and kept at logic 1 to fetch the value stored in the cell. The write operation also requires clk and write enable (WR_En) to be at logic 1 to achieve successful modification to the stored information in the cell.

5.3 6T SRAM Functionality

SRAM working consists of three operating modes: hold, read, and write. The hold state keeps the data inside the positive feedback with the help of a weak cross-coupled inverter. The cross-coupling provides immunity to the external world noise that can cause stored information to flip. To achieve stability and writability, the noise margins are defined for all the modes of operation. These are known as hold margin, read margin, and write margin. The static noise margin (SNM) determines the amount of noise voltage that can be applied before the stable state is lost. In this thesis, the main focus was to analyze the read and right margin of the SRAM cell operating on a high frequency. The aforementioned margins were compared for multi-threshold and a multi-corner transistor to present the robustness of the designed SRAM bit cell [41].

The read operation starts with pre-charging the bit line (BL) and bit bar line (BB) by using pre-charge transistors shown in figure 5.14. Assuming Q is initially at logic "0" before the operation starts and this operation is read "0" operation. The word line (WL) is raised to VDD that eventually turns on both the access transistors M7 and M3 shown in figure 5.7. The current starts flowing through the left access transistor M7 and the voltage at the internal node Q begins to change. Due to the presence of logic "1" at the internal node QB the pull down transistor M1 turns and starts discharge the bitline (BL) pre-charged voltage. During the pulling down process, the transistor M1 was found to be in the linear region of operation while the access transistor M7 is in saturation mode. As the voltage decreases at the bitline node, the bitline and bitbar line voltages are sensed by the sense amplifier. The sense amplifier detects the change in the bitline voltage and compares it to bitbar line voltage. In the read "0" operation, the bitline voltage decreases due to the discharge through the pull down transistor while the bitbar line voltage remains the same. This difference in the voltage of the pre-charge nodes is detected as the stored logic "0" information inside the cell. The constrain for the read operation is not to flip the

stored logic level in the bit cell. This condition is ensured by making the pull down transistor stronger than the access transistors that avoid another pull down transistor M0 to turn on. Figure 5.12 shows the read margin circuit used to evaluate the read SNM for multiple corners specified in table 5.3, 5.4, 5.5, and 5.6 for different threshold voltage flavors.

The write "1" operation is not possible by forcing Q through the access transistor M7 on the account of the read stability. Hence, this operation is achieved by pulling the Q_bar to logic "0" through the access transistor M3 as shown in figure 5.7. The operation starts by forcing the bitbar line to low voltage. The logic "1" stored at the internal node Q_bar is forced to a logic "0" by turning off the pull up transistor M6. The transistor M6 opposes this operation; thus, M6 must be weaker than the access transistor M3. The writability constraint requires the pullup: access of 1:2 sizing ratio. Figure 5.13 presents the testbench used for the SNM simulation and Figure 5.15 depicts the simulated write margin curve on the Cadence Spectre simulator tool. Further, tables from 5.3 to 5.6 compare the write SNM on various operating conditions. Also, figure 5.11 shows the functionality simulation of 6T SRAM cell with the rise and fall time of 1ps.

Table 5.3.
Read & Write SNM for SLVt transistors

SLVt	V_{DD}(V)	$Temp$	SNM_{RD}(mV)	SNM_{WR}(mV)
SS	0.63	100	0.3381	0.6038
TT	0.7	25	0.1864	0.3000
FF	0.77	0	0.4173	0.2958

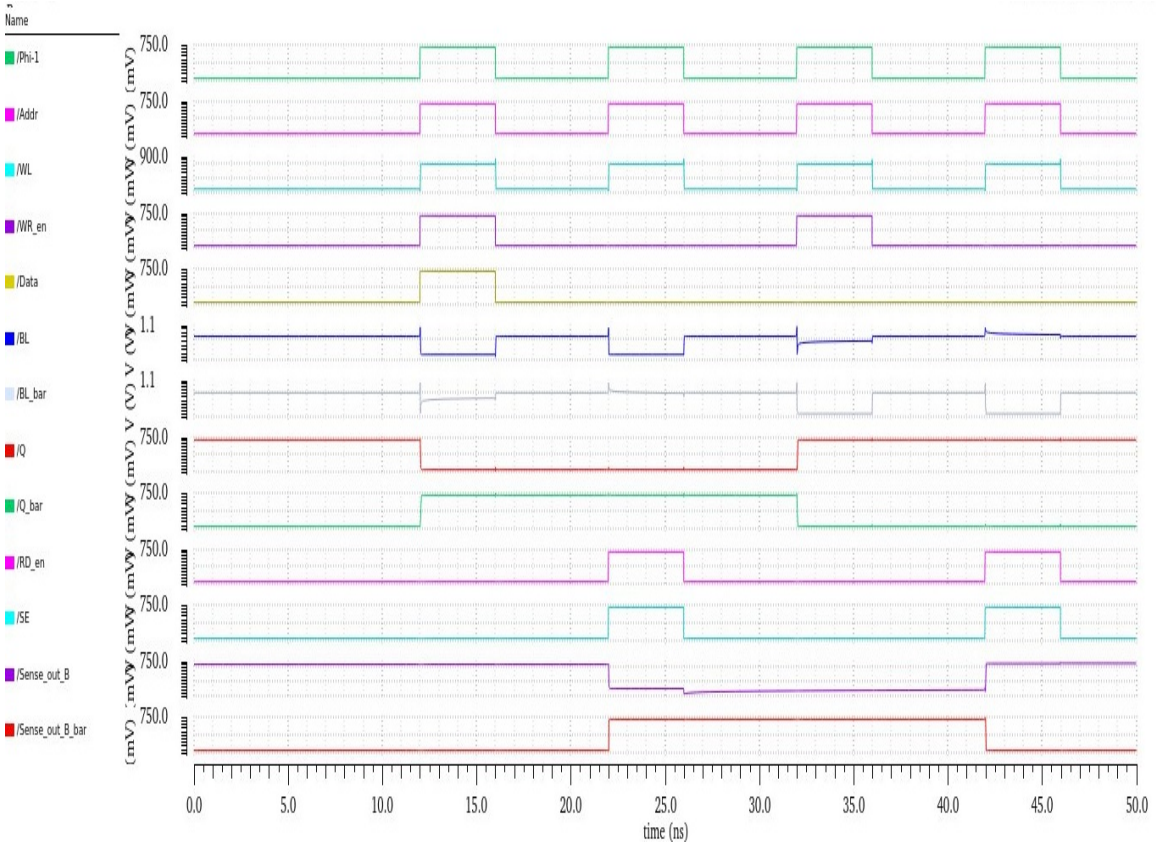

Fig. 5.11. 6T SRAM read and write operations.

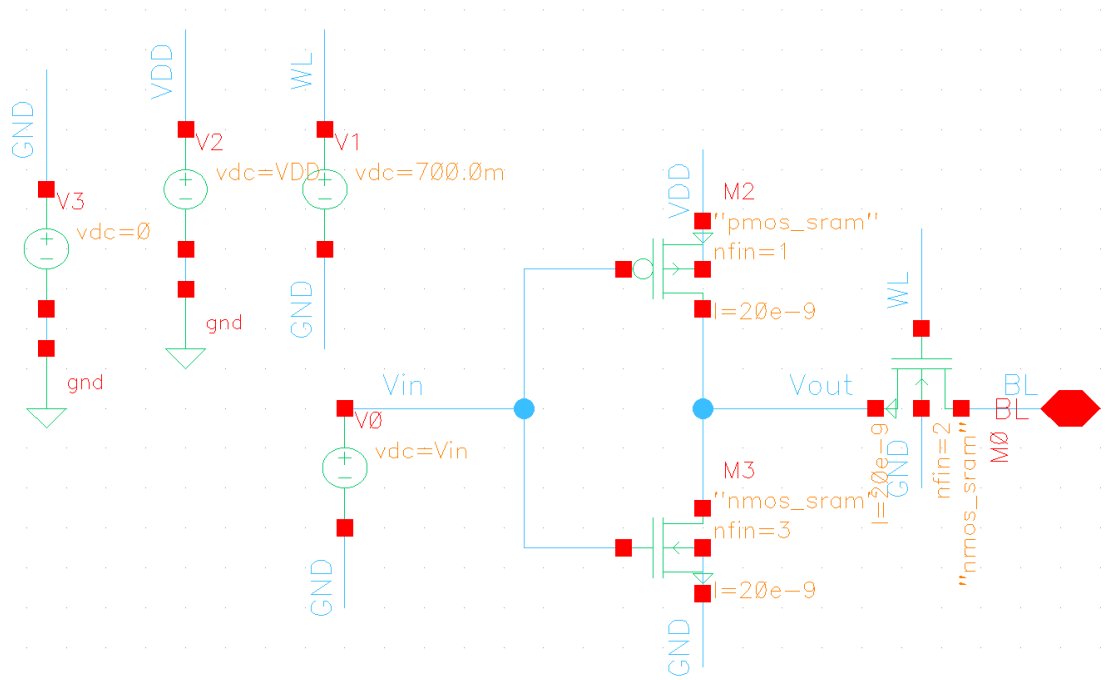

Fig. 5.12. Read SNM circuit.

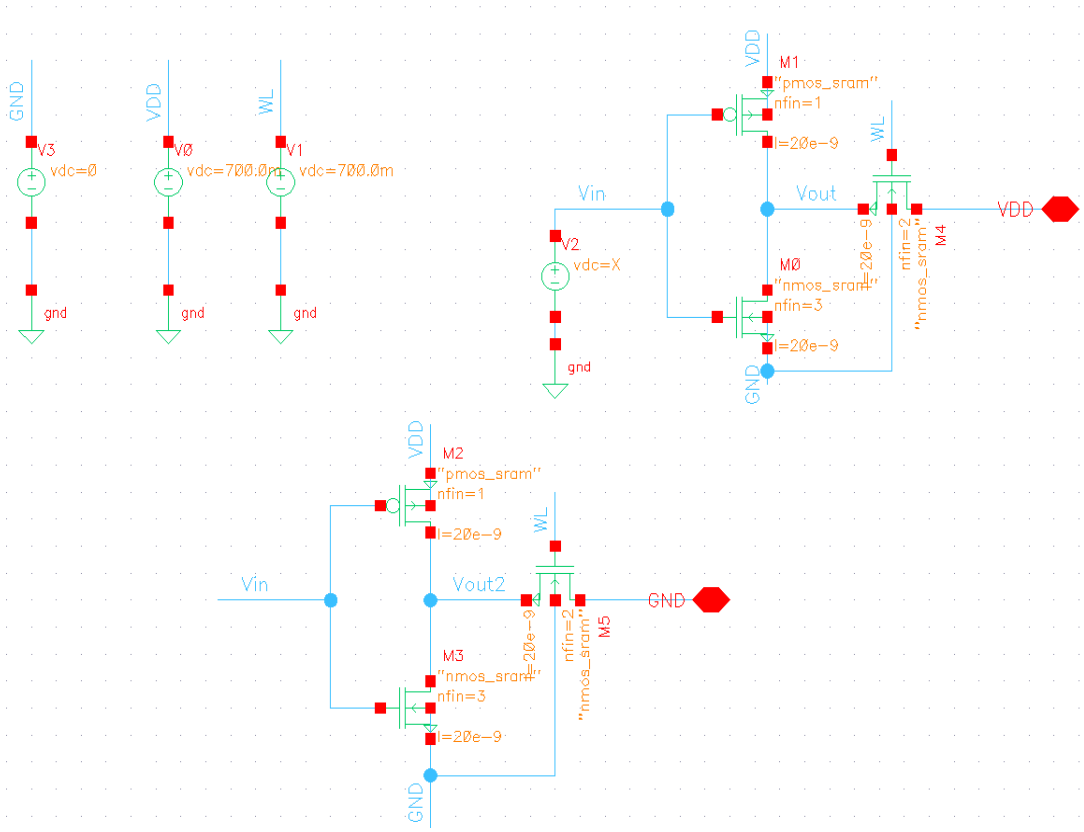

Fig. 5.13. Write SNM circuit.

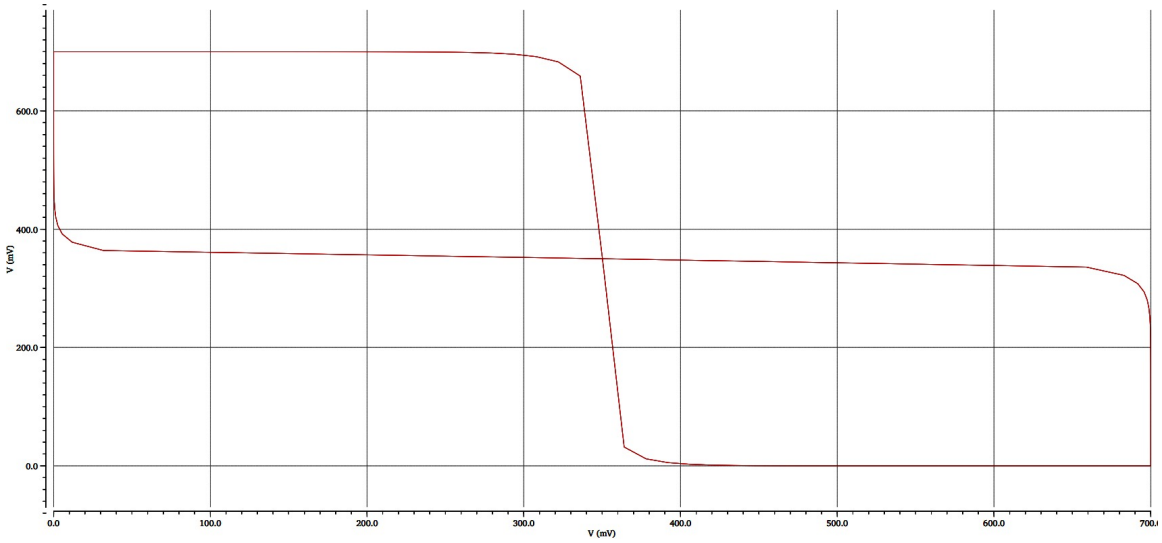

Fig. 5.14. Read static noise margin.

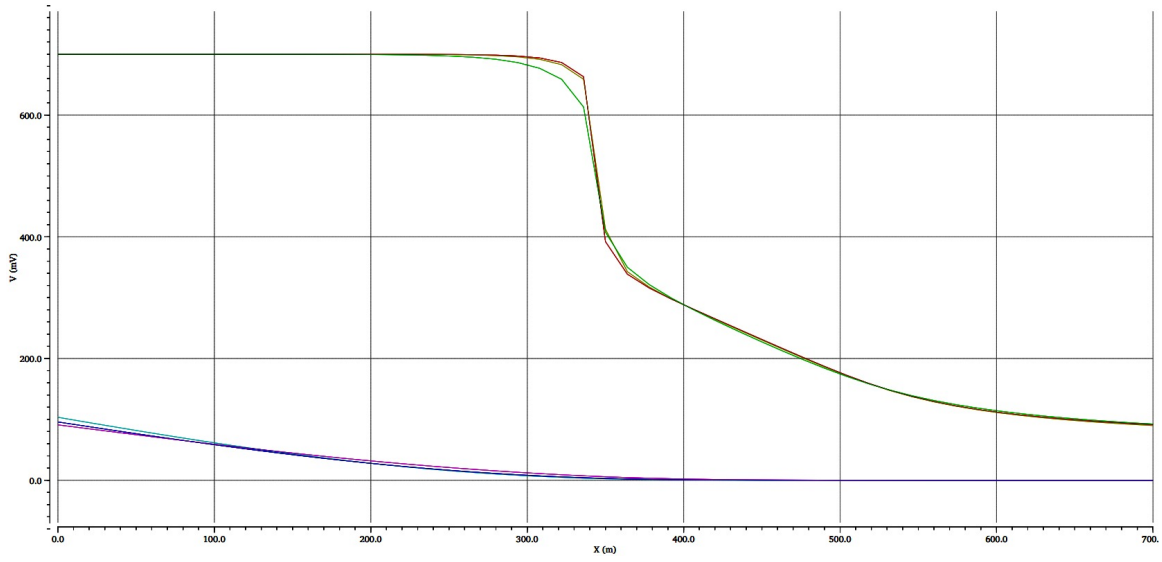

Fig. 5.15. Write static noise margin.

Table 5.4.
Read & Write SNM for LVt transistors

LVt	V_{DD}(V)	$Temp$	SNM_{RD}(mV)	SNM_{WR}(mV)
SS	0.63	100	0.1983	0.6143
TT	0.7	25	0.2277	0.6127
FF	0.77	0	0.2446	0.6033

Table 5.5.
Read & Write SNM for RVt transistors

RVt	V_{DD}(V)	$Temp$	SNM_{RD}(mV)	SNM_{WR}(mV)
SS	0.63	100	0.2263	0.6368
TT	0.7	25	0.2679	0.6307
FF	0.77	0	0.2899	0.6212

Table 5.6.
Read & Write SNM for SRAM Vt transistors

SRAM Vt	V_{DD}(V)	$Temp$	SNM_{RD}(mV)	SNM_{WR}(mV)
SS	0.63	100	0.3428	0.6761
TT	0.7	25	0.0150	0.6761
FF	0.77	0	0.4025	0.3470

6. SYSTEM LEVEL DESIGN

The datapath elements are the most quantifying designs to judge the performance of any chip. As the technology advanced and moved towards the sub-micron processes, the control over the parameters' speed, power, and area became more complex. In the last few years, ASIC chips showed high productivity but delay and power became the concerning factors of designs. The FinFET is another advancement in transistor technology. This thesis model a 32 bit ALU design that is optimized on 1 GHz with 16 functions based on the 7nm FinFET process from ASAP 7nm process design kit [7]. The design is targeted for low power applications through ASIC methodology and achieved an overall average power of 1 mW per sq. mm. The design flow was developed for cutting edge 7nm FinFET by integrating the industry standard tools from vendors Synopsys and Cadence for frontend and backend design respectively. This article presents the delay and power values including pre-layout and post-layout phases with noble 7nm FinFET technology.

6.1 Digital Design Methodology

Digital circuits usually consist of datapath elements, memory elements, and control structures. The datapath elements are involved in arithmetic and logic operations inside CPUs. Another important part of the CPU is the memory element, that is also addressed array subsystems and involved in load and store operations to access the data. Lastly, control structures are synthesized by writing behavioral HDL. The datapath components are one of the important parts of any design and they decide the maximum frequency on which a design is functional. They are also important during delay calculation and power estimation of any system. Generally, datapath operators include adders, multipliers, shifters, and comparator circuits. Application Specific

Integrated Circuits (ASICs) designs are synthesized by writing a behavioral description that facilitates the implementation flow. ASIC design flow allows designers to model the RTL description efficiently and provides freedom of choice in implementation techniques considering the rules of HDL description [42]. The term ASIC simply refers to an IC that has been designed for a particular application and this kind of ICs currently defines a portion of the semiconductor market. The semiconductor market also includes memories, microprocessors, and field programmable gate arrays (FPGAs). The ASIC tool vendors such as Synopsys and Cadence offers complete design flows know as Digital Design Flow. There is some requirement to fulfill to achieve a highly efficient design. They are ASIC tools integration, standard cell libraries for the process, and a particular design implementation technique. Collectively, they come with an ASIC design kit. ASICs are designed at the register-transfer level (RTL) in Verilog or VHDL, specifying the flow of data between registers and the state to store in registers. Commercial EDA tools are used to map the higher level RTL description to standard cells in an ASIC library, and then place the cells and route wires [22]. It is much easier to migrate ASIC designs to new process technology, compared to custom designs that have been optimized for a specific process at the gate or transistor-level.

6.2 Design Description

The ALU was designed for 16 operations that are defined in Table 6.1. This ALU takes two 32 bit operands as inputs, performs an operation on the operands selected by select line $func$, and gives outputs at alu_out port of the design. The design is valid for integer values as the goal of the design was to estimate the power and delay values. Figure 6.3 shows the module level schematic of the design.

6.3 Library Development

Library characterization data can be stored in a text file in the Liberty (.lib) format [25]. The Library Compiler tool reads the description of an ASIC library from

Table 6.1.
Functions of arithmetic and logic unit

Function Name	**Expression**
Addition	a+b
Subtraction	a-b
2's complement	$\sim$ a + 1'b1
Multiplication	a*b
Bitwise Left Shift	$a << 1$
Bitwise Right Shift	$a >> 1$
Bitwise OR	$a\|b$
Bitwise AND	a&b
Bitwise XOR	aˆb
Bitwise XNOR	$\sim$ (aˆb)
Bitwise NAND	$\sim$(a&b)
Bitwise NOR	$\sim$(a|b)
Rotate Left	a[30:0],a[31]
Rotate Right	a[0],a[31:1]
Greater Than	a>b
Equivalence Check	a=b

the .lib file and compiles the description into an internal database (.db file format) as shown in figure 6.1. The compiled library database can then be used for timing, power, and noise analysis with compatible synthesis, place and route, static timing analysis, and verification tools. A logical library contains mainly two things:

- Cell descriptions define each individual component in the ASIC technology.
- Environment descriptions contain information about the technology node that is not unique to individual components. This section also contains information about the effects of operating conditions on the technology, values of the com-

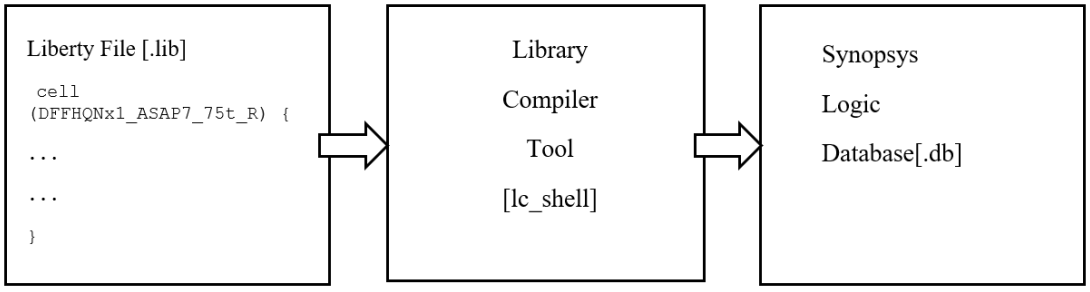

Fig. 6.1. Library Compiler to generate db files.

ponents of delay scaling equations, statistical data of interconnect estimation, and default cell attributes.

Optimization tools use the timing parameters and environment attributes described in a logic library to calculate the timing delays for your designs. The timing parameters and environmental attributes depend on the delay model. The following TCL script is written to convert liberty files to Synopsys database (.db) format.

```
#Read all liberty files to a TCL list my_lib.
set my_lib [glob ./NLDM/asap7sc7p5t_*]
#Interate over each .lib of list to read and write a .db file.
foreach ele $my_lib {
set lwr_idx [string last / $ele]
set upr_idx [string last .lib $ele]
set str [string range $ele [expr $lwr_idx + 1] [expr $upr_idx - 1]]
echo "$str"
read_lib $ele
write_lib $str  -format db -output ./NLDM_db/${str}.db
}
```

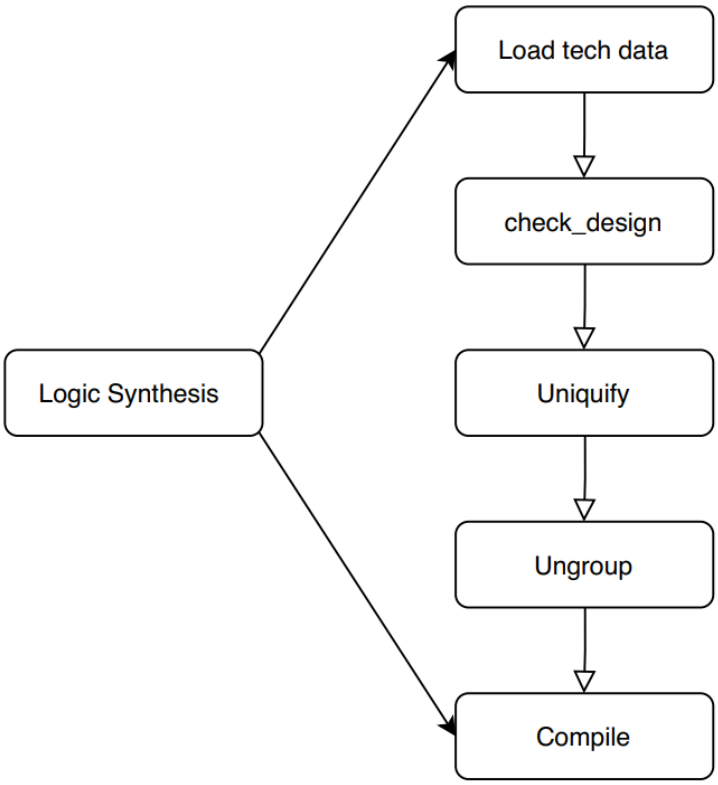

Fig. 6.2. RTL synthesis approach.

6.4 Logic Synthesis

Generally, logic synthesis can be expressed as a combination of translation, mapping, and optimization [24]. This step mapped all behaviors description into a structural gate-level netlist [43]. The RTL synthesis approach is shown in figure 6.2. Synthesis can be executed in different types depending upon our requirements. The Design Ware (DW) datapath elements were automatically picked up from the tool's library for each operation and optimized on provided design constraints [44].

6.4.1 Synopsys Design Constraints (SDC)

The SDC format is utilized to specify the design intent, including the area, power, and timing constraints for the design [45]. The design constraints are broadly divided

into two parts: Logical Design Rule Constraints and Optimization Constraints. The logical DRCs are defined in the liberty file and limit the cells during the logical synthesis to achieve correct functionality. In this design, these constraints are automatically picked from the NLDM liberty file during synthesis [12]. On the other hand, the optimization constraints start from defining a clock for the design and further adding more complicated constraints on the basis of the defined clock period.

Time budgeting is the start point of the optimization constraints development process. The whole design is divided into three path groups: Input to Reg, Reg to Reg, and Reg to Output [24]. The constraint *set_input_delay* was used to constrain all the input ports of the design with an input arrival time of 600 ps for the setup timing analysis. The concept of a virtual clock was used to associate the input delay to the ports. Input transition models the propagated signal transition during Logic Synthesis and is assigned to all the input ports using *set_input_transition* command. Moreover, to constraint all the output ports with 2fF load capacitance, *set_load* command was used. Below is the set of SDC commands that were used to constrain the ALU design for synthesis. Command *set_clock_uncertainty* is used to model the clock jitter and clock skew effects to the ideal clock during the synthesis [46]. It also includes some margin that is considered to deal with any unexpected change in the later design implementation stages. As the design uses a single clock for implementation, the clock latency terms will cancel each other and can be ignored for a single clock design [47].

After applying these constraints, the following two clocks were generated. The clock CLK is a master clock with periodicity 1000 ps (1 ns) and associated with the CLK port of the design whereas the virtual clock $VCLK$ with the same period as the master clock to set the input delay for the design.

```
create_clock -period 1000 -name CLK [get_ports clk]
set_clock_uncertainty -setup 15 [get_clock CLK]
set removed_ports [remove_from_collection [all_inputs] \
[get_ports clk]]
set data_input_ports [remove_from_collection $removed_ports \
```

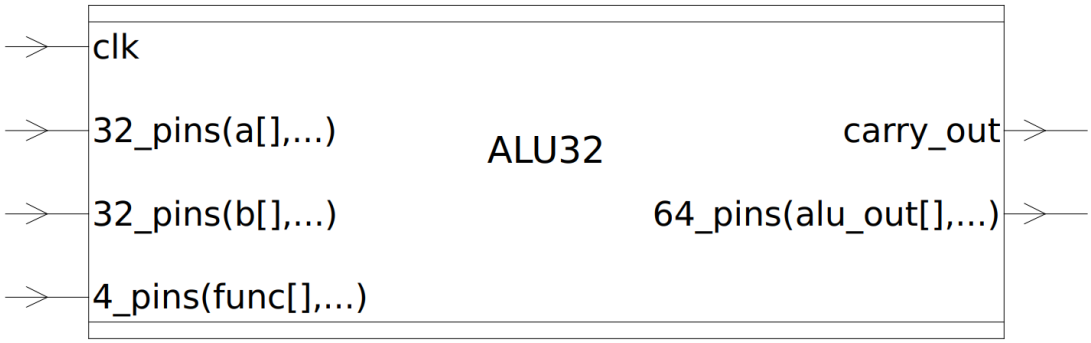

Fig. 6.3. Schematic design.

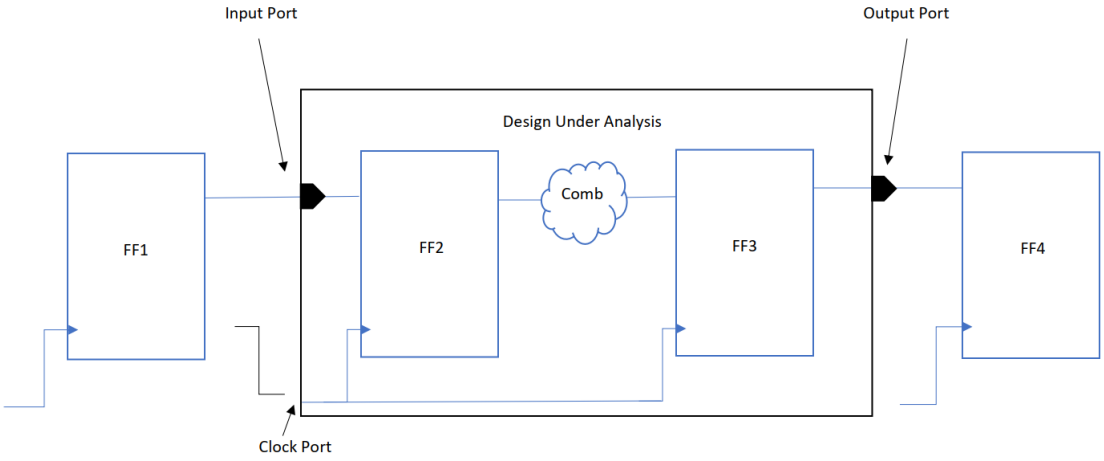

Fig. 6.4. Timing paths in design.

```
[get_ports func[*]]]
create_clock -period 1000 -name VCLK
set_input_delay -max 600 $data_input_ports -clock VCLK
set_input_transition -max 8 [get_ports $data_input_ports]
set_load -max 2 [get_ports [all_outputs]]

****************************************
Report : clocks
Design : ALU32
Version: O-2018.06-SP5-2
Date   : Tue Oct 13 16:53:06 2020
****************************************
Attributes:
    f - fix_hold
    p - propagated_clock
    G - generated_clock
    g - lib_generated_clock
Clock          Period   Waveform            Attrs     Sources
------------------------------------------------------------------------
CLK           1000.00   {0 500}                       {clk}
VCLK          1000.00   {0 500}                       {}
------------------------------------------------------------------------
```

6.4.2 Optimization Approaches

Design compiler uses various optimization techniques. The techniques used in this design is listed below:

- Prioritizing Logical DRCs
- Uniquification
- Datapath Sharing

- Synthetic Operators
- Automatic Ungrouping

6.4.3 LVt TT Synthesis Results

The logic synthesis was performed on all possible threshold voltage and corner combinations. The exhaustive synthesis captured the timing and power QoRs that are compared in further tables. First, the Lvt TT corner synthesis result is elaborately presented for timing and power reports generated from the Design Compiler. It starts with the operating condition report used for this synthesis run followed by the timing and power reports for the same operating condition.

```
Operating Condition Name : PVT_0P7V_25C
Library : asap7sc7p5t_22b_SEQ_LVT_TT_170906
Process :   1.00
Temperature :  25.00
Voltage :   0.70
```

The following reports show the input to the reg path of the design.

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : ALU32
Version: L-2016.03-SP1
Date   : Wed Oct 21 01:54:10 2020
****************************************

Operating Conditions: PVT_0P7V_25C
```

```
Library: asap7sc7p5t_22b_OA_LVT_TT_170906
Wire Load Model Mode: top
  Startpoint: a[31] (input port clocked by VCLK)
  Endpoint: a_in_reg[31]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------
  clock VCLK (rise edge)                             0.00       0.00
  clock network delay (ideal)                        0.00       0.00
  input external delay                             600.00     600.00 f
  a[31] (in)                                         0.00     600.00 f
  U2745/Y (INVxp33_ASAP7_75t_L)                      7.82     607.82 r
  a_in_reg[31]/D (DFFHQNx1_ASAP7_75t_L)              0.00     607.82 r
  data arrival time                                           607.82

  clock CLK (rise edge)                           1000.00    1000.00
  clock network delay (ideal)                        0.00    1000.00
  clock uncertainty                                -15.00     985.00
  a_in_reg[31]/CLK (DFFHQNx1_ASAP7_75t_L)            0.00     985.00 r
  library setup time                                -6.96     978.04
  data required time                                          978.04
  -----------------------------------------------------------------
  data required time                                          978.04
  data arrival time                                          -607.82
  -----------------------------------------------------------------
  slack (MET)                                                 370.22
```

The following report describes the max path in the design for the setup analysis and ensures that the design work on the 1GHz clock frequency. The value of the slack for this report is positive 0.51 ps and hence met.

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : ALU32
Version: L-2016.03-SP1
Date   : Wed Oct 21 01:50:44 2020
****************************************
Operating Conditions: PVT_0P7V_25C
Library: asap7sc7p5t_22b_OA_LVT_TT_170906
Wire Load Model Mode: top

  Startpoint: b_in_reg[11]
              (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: alu_value_reg[63]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max
  -----------------------------------------------------------------
  Point                                              Incr       Path
  -----------------------------------------------------------------
  clock CLK (rise edge)                              0.00       0.00
  clock network delay (ideal)                        0.00       0.00
```

b_in_reg[11]/CLK (DFFHQNx1_ASAP7_75t_L)	0.00	0.00	r
b_in_reg[11]/QN (DFFHQNx1_ASAP7_75t_L)	47.81	47.81	f
U1602/Y (XNOR2xp5_ASAP7_75t_L)	21.38	69.20	r
U1605/Y (NOR2xp33_ASAP7_75t_L)	9.93	79.13	f
U1004/Y (HB1xp67_ASAP7_75t_L)	61.32	140.45	f
U1606/Y (NAND2xp33_ASAP7_75t_L)	22.50	162.96	r
U1607/Y (OAI21xp33_ASAP7_75t_L)	19.87	182.83	f
U1616/Y (INVxp33_ASAP7_75t_L)	15.36	198.19	r
U1617/Y (AND2x2_ASAP7_75t_L)	14.52	212.71	r
U1618/Y (AND2x2_ASAP7_75t_L)	12.88	225.59	r
U1619/Y (AND2x2_ASAP7_75t_L)	12.13	237.73	r
mult_x_1/U1087/CON (FAx1_ASAP7_75t_L)	8.42	246.14	f
U2700/Y (INVxp67_ASAP7_75t_L)	12.21	258.35	r
mult_x_1/U1078/SN (FAx1_ASAP7_75t_L)	32.63	290.98	f
mult_x_1/U1075/CON (FAx1_ASAP7_75t_L)	23.93	314.90	r
mult_x_1/U1075/SN (FAx1_ASAP7_75t_L)	13.81	328.71	f
mult_x_1/U1073/CON (FAx1_ASAP7_75t_L)	14.48	343.19	r
mult_x_1/U1073/SN (FAx1_ASAP7_75t_L)	7.19	350.38	f
U1154/Y (INVxp33_ASAP7_75t_L)	11.19	361.57	r
U3253/Y (NOR2xp33_ASAP7_75t_L)	12.55	374.13	f
U3293/Y (NOR2xp33_ASAP7_75t_L)	10.61	384.74	r
U3295/Y (AOI21xp5_ASAP7_75t_L)	8.10	392.84	f
U776/Y (OAI21xp5_ASAP7_75t_L)	13.57	406.40	r
U1237/Y (AOI21xp5_ASAP7_75t_L)	14.55	420.96	f
U771/Y (OAI21x1_ASAP7_75t_L)	13.25	434.20	r
U770/Y (AOI21x1_ASAP7_75t_L)	10.41	444.62	f
U1366/Y (OAI21x1_ASAP7_75t_L)	12.07	456.68	r
U3417/Y (AOI21x1_ASAP7_75t_L)	10.41	467.10	f
U3431/Y (OAI21x1_ASAP7_75t_L)	12.07	479.16	r

U3453/Y (AOI21x1_ASAP7_75t_L)	10.42	489.58	f
U1365/Y (OAI21x1_ASAP7_75t_L)	12.09	501.67	r
U3486/Y (AOI21x1_ASAP7_75t_L)	10.47	512.14	f
U3504/Y (OAI21x1_ASAP7_75t_L)	12.08	524.22	r
U3511/Y (AOI21x1_ASAP7_75t_L)	10.47	534.69	f
U758/Y (OAI21x1_ASAP7_75t_L)	12.08	546.77	r
U780/Y (AOI21x1_ASAP7_75t_L)	9.23	556.00	f
U779/Y (OAI21xp5_ASAP7_75t_L)	13.49	569.48	r
U927/Y (AOI21xp5_ASAP7_75t_L)	14.63	584.11	f
U757/Y (OAI21x1_ASAP7_75t_L)	13.26	597.37	r
U778/Y (AOI21x1_ASAP7_75t_L)	10.47	607.83	f
U777/Y (OAI21x1_ASAP7_75t_L)	12.08	619.92	r
U761/Y (AOI21x1_ASAP7_75t_L)	10.47	630.38	f
U760/Y (OAI21x1_ASAP7_75t_L)	12.08	642.47	r
U763/Y (AOI21x1_ASAP7_75t_L)	10.47	652.93	f
U762/Y (OAI21x1_ASAP7_75t_L)	10.61	663.54	r
U915/Y (AOI21xp5_ASAP7_75t_L)	13.71	677.25	f
U773/Y (OAI21x1_ASAP7_75t_L)	13.13	690.37	r
U772/Y (AOI21x1_ASAP7_75t_L)	10.47	700.84	f
U781/Y (OAI21x1_ASAP7_75t_L)	12.08	712.92	r
U756/Y (AOI21x1_ASAP7_75t_L)	10.47	723.39	f
U766/Y (OAI21x1_ASAP7_75t_L)	10.20	733.59	r
U911/Y (AO22x1_ASAP7_75t_L)	16.47	750.06	r
U910/Y (AO22x1_ASAP7_75t_L)	15.90	765.95	r
U775/Y (NAND2xp5_ASAP7_75t_L)	5.66	771.61	f
U774/Y (NAND2xp5_ASAP7_75t_L)	10.30	781.91	r
U765/Y (AO22x2_ASAP7_75t_L)	15.38	797.29	r
U908/Y (AO22x1_ASAP7_75t_L)	14.89	812.18	r
U1493/Y (AO22x1_ASAP7_75t_L)	16.07	828.25	r

```
U3611/Y (AO22x2_ASAP7_75t_L)                    14.66     842.91 r
U711/Y (INVx1_ASAP7_75t_L)                       5.31     848.22 f
U3614/Y (OAI21x1_ASAP7_75t_L)                    9.19     857.41 r
U764/Y (NAND2xp5_ASAP7_75t_L)                    6.03     863.44 f
U736/Y (NAND2xp5_ASAP7_75t_L)                   10.35     873.79 r
U3619/Y (AO22x2_ASAP7_75t_L)                    15.68     889.47 r
U3622/Y (AO22x2_ASAP7_75t_L)                    13.89     903.36 r
U3625/Y (AO22x2_ASAP7_75t_L)                    13.64     917.01 r
U1492/Y (AO22x1_ASAP7_75t_L)                    15.40     932.40 r
U3630/Y (AO22x2_ASAP7_75t_L)                    14.63     947.03 r
U735/Y (AOI22xp5_ASAP7_75t_L)                    7.55     954.58 f
U3637/Y (XOR2xp5_ASAP7_75t_L)                   12.86     967.44 f
U782/Y (AOI21xp5_ASAP7_75t_L)                    7.94     975.39 r
alu_value_reg[63]/D (DFFHQNx1_ASAP7_75t_L)       0.00     975.39 r
data arrival time                                          975.39

clock CLK (rise edge)                         1000.00    1000.00
clock network delay (ideal)                      0.00    1000.00
clock uncertainty                              -15.00     985.00
alu_value_reg[63]/CLK (DFFHQNx1_ASAP7_75t_L)     0.00     985.00 r
library setup time                              -9.10     975.90
data required time                                         975.90
-----------------------------------------------------------------
data required time                                         975.90
data arrival time                                         -975.39
-----------------------------------------------------------------
slack (MET)                                                  0.51
```

The report shown below is the min report generated for the hold analysis. This also shows positive slack value means met the requirement for the contamination delay through the combinational logic sitting between flop to flop path.

```
****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : ALU32
Version: L-2016.03-SP1
Date   : Wed Oct 21 01:50:57 2020
****************************************
Operating Conditions: PVT_0P7V_25C
Library: asap7sc7p5t_22b_OA_LVT_TT_170906
Wire Load Model Mode: top

  Startpoint: func_in_reg[3]
              (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: alu_value_reg[0]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: min
  -----------------------------------------------------------------
  Point                                              Incr       Path
  -----------------------------------------------------------------
  clock CLK (rise edge)                              0.00       0.00
  clock network delay (ideal)                        0.00       0.00
  func_in_reg[3]/CLK (DFFHQNx1_ASAP7_75t_L)          0.00       0.00 r
  func_in_reg[3]/QN (DFFHQNx1_ASAP7_75t_L)          34.03      34.03 r
```

```
  U3007/Y (AOI21xp33_ASAP7_75t_L)                    8.78      42.82 f
  alu_value_reg[0]/D (DFFHQNx1_ASAP7_75t_L)          0.00      42.82 f
  data arrival time                                            42.82

  clock CLK (rise edge)                              0.00       0.00
  clock network delay (ideal)                        0.00       0.00
  alu_value_reg[0]/CLK (DFFHQNx1_ASAP7_75t_L)        0.00       0.00 r
  library hold time                                  1.14       1.14
  data required time                                            1.14
  -----------------------------------------------------------------
  data required time                                            1.14
  data arrival time                                           -42.82
  -----------------------------------------------------------------
  slack (MET)                                                  41.67
```

The following report shows the power consumption in the ALU design that includes static and dynamic power. The static power consumed by design is total power consumption is 0.4867 mW

```
Operating Conditions: PVT_0P7V_25C
Library: asap7sc7p5t_22b_OA_LVT_TT_170906
Wire Load Model Mode: top
Global Operating Voltage = 0.7
Power-specific unit information:
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ps
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW
```

```
  Cell Internal Power  = 256.1146 uW   (53%)
  Net Switching Power  = 227.7242 uW   (47%)
                         ---------
Total Dynamic Power    = 483.8388 uW  (100%)

Cell Leakage Power     =   2.8704 uW

               Internal  Switching  Leakage       Total
Power Group    Power     Power      Power         Power   (%)
------------------------------------------------------------------
io_pad         0.0000    0.0000     0.0000        0.0000  (0.00%)
memory         0.0000    0.0000     0.0000        0.0000  (0.00%)
black_box      0.0000    0.0000     0.0000        0.0000  (0.00%)
clock_network  0.0000    0.0000     0.0000        0.0000  (0.00%)
register       0.1211    2.2041e-02 2.9219e+05    0.1434  (29.46%)
sequential     0.0000    0.0000     0.0000        0.0000  (0.00%)
combinational  0.1351    0.2057     2.5782e+06    0.3433  (70.54%)
------------------------------------------------------------------
Total          0.2561mW  0.2277mW   2.8704e+06 pW  0.4867 mW
```

The following report presents the area reported for the design after technology mapping and optimization.

```
****************************************
Report : area
Design : ALU32
Version: L-2016.03-SP1
Date   : Sun Nov  1 16:48:45 2020
****************************************
```

```
Library(s) Used:
    asap7sc7p5t_22b_SIMPLE_LVT_TT_170906
    asap7sc7p5t_22b_OA_LVT_TT_170906
    asap7sc7p5t_22b_AO_LVT_TT_170906
    asap7sc7p5t_22b_INVBUF_LVT_TT_170906
    asap7sc7p5t_22b_SEQ_LVT_TT_170906

Number of ports:                          134
Number of nets:                          3568
Number of cells:                         3211
Number of combinational cells:           3079
Number of sequential cells:               132
Number of macros/black boxes:               0
Number of buf/inv:                        423
Number of references:                      44

Combinational area:               4939.004072
Buf/Inv area:                      297.665284
Noncombinational area:             615.859177
Macro/Black Box area:                0.000000
---------------------------------------------
Total cell area:                  5554.863249
---------------------------------------------
```

6.4.4 Multi-corner Synthesis Results Comparison

The ALU behavioral RTL description was synthesized on various corners that come with the library. To compare results accurately, the same design constraints were applied during the synthesis with the same optimization approaches. Each threshold

voltage flavor was constrained for three PVT conditions specified in table 6.2, 6.3, and 6.4. The tabulated results show the hold timing slack (Min Slack), setup timing slack (Max Slack), and the total power consumption. The current version of the library contains only a single physical view in GDSII format for physical implementation purposes. Hence, the post-layout area of each corner must be the same. This is the reason for not comparing areas in tabulated synthesis results. The performance optimization trades with the area and power to achieve positive slack for timing closure. The timing and power QoRs are compared also compared with the 15nm Nan-Gate library in table 6.5. Synthesis results show the power consumed by 7nm is almost one-third of the power consumed by 15nm.

Table 6.2.
Comparison of synthesis results for multi-corner LVt libs

LVt Libs	V_{DD}(V)	$Temp$	$MinSlack$(ps)	$MaxSlack$(ps)	P_{total}(mW)
SS	0.63	100	43.86	1.10	0.4108
TT	0.7	25	41.67	0.51	0.4867
FF	0.77	0	31.64	0.07	0.6828

Table 6.3.
Comparison of synthesis results for multi-corner RVt libs

RVt Libs	V_{DD}(V)	$Temp$	$MinSlack$(ps)	$MaxSlack$(ps)	P_{total}(mW)
SS	0.63	100	63.43	0.29	0.3425
TT	0.7	25	44.34	0.41	0.4390
FF	0.77	0	37.23	0.08	0.6020

Table 6.4.
Comparison of synthesis results for multi-corner SLVt libs

SLVt Libs	V_{DD}(V)	$Temp$	$MinSlack$(ps)	$MaxSlack$(ps)	P_{total}(mW)
SS	0.63	100	34.77	0.04	0.7375
TT	0.7	25	32.49	0.13	0.6238
FF	0.77	0	28.46	1.21	0.8739

Table 6.5.
Comparison of synthesis results for multi-corner 15nm Nan-Gate libs

Process	V_{DD}(V)	$Temp$	$MinSlack$(ps)	$MaxSlack$(ps)	P_{total}(mW)
SS	0.72	100	274.00	12.58	2.8512
TT	0.80	25	247.62	12.10	1.3140
FF	0.88	0	261.02	14.77	1.6696

6.5 Formal Verification

This step was executed on Synopsys Formality and this process is also known as Logic Equivalence Check. In this phase of the design flow, the gate-level netlist is considered as an implemented design/container whereas the behavioral description is considered as a reference design/container. Formality does not guarantee meeting the design specifications but it assures the Boolean Equivalence from the reference design. During this check, the ALU design went through the steps match, verify, and debug. As the design did not show any functional issues after synthesis, the gate-level netlist was considered to be correct for physical implementation [48].

6.6 Physical Design

Any ASIC design implementation required different kinds of libraries during physical implementation. Most libraries are consist of a physical database, timing database,

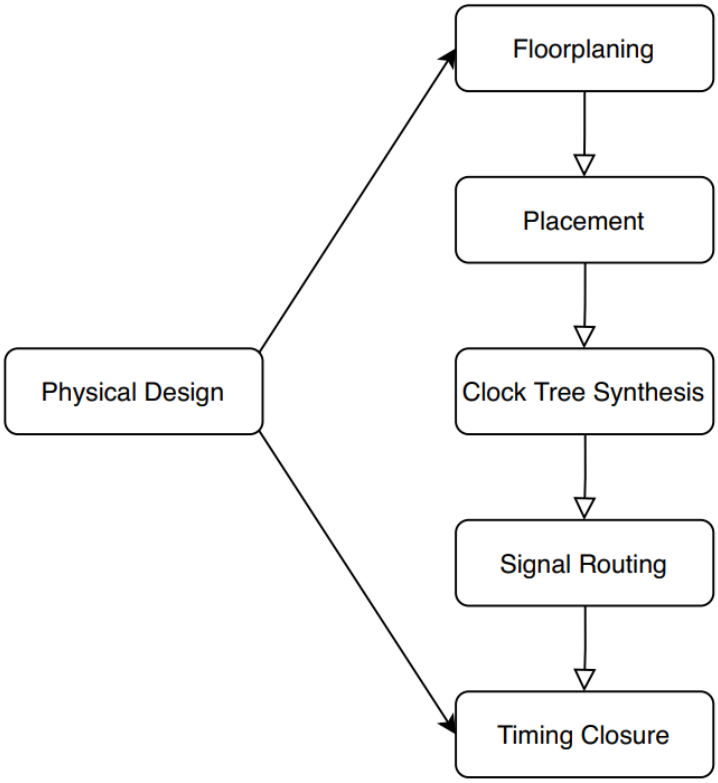

Fig. 6.5. Physical design approach.

transistor-level spice description, and functional models. They are generated using tools from Synopsys and Cadence. Libraries are considered as one of the most critical parts of the ASIC design. They decide the accuracy of downstream physical design steps, level of optimization, and success in fabrication. The physical implementation approach is shown in figure 6.5.

6.6.1 Floorplan

Floorplanning is the art of any physical design. A well-planned floorplan increases the feasibility of further downstream physical design steps while maintaining higher performance and optimum area. Floorplanning deals with challenging tasks such as placement of I/O pads and macros as well as the creation of power and ground

structures. The proper technology database preparation is required before starting the floorplan. Entire floorplanning converts the logical blocks into physical form and assigns silicon real-state to them. In this design, the floorplan is created with a 1.0 aspect ratio (square) and core to die difference of 10um from all sides. The utilization is a term that leads to some serious issues like congestion. Power routing should be implemented on higher metal layers to avoid congestion problems and the utilization should be 0.7 as it explained efficiently in terms of wire length used in the design.

The logical design rule constraints are also required in physical design that comes with the logical libraries of standard cells [49]. There are three types of logical design rule constraints: Maximum fanouts, Maximum transitions, Maximum capacitance. They are defined in section 2.7. These logical design rule constraints are mainly achieved by performing physical synthesis at various stages of physical design.

6.6.2 Placement

The aim of the standard cell placement step is to map ASIC design standard cells to positions of the created core area that is defined by site array generated during floorplan. The standard cells must be placed on the site rows such that the signal routing can be performed efficiently by taking care of overall timing and congestion requirements [50]. Standard cell placement of a design has always been a major step to achieve optimum area usage, less routing congestion, and good timing behavior in any physical implementation. Almost all of today's physical design tools form various EDA vendors use various NP-complete algorithms to place standard cells automatically and route them [49]. The placement algorithms are very complex and are being modified frequently to converge design at better QoR. In modern sub-nanometer processes, the routing channels are extremely dense and need extra cautious signal routing to eliminate the congestion problem. During placement, the global route cell mechanism is used to estimate the overflow of tracks in a specific region to present the congestion maps in front of designers. The overall objective of most place-and-route

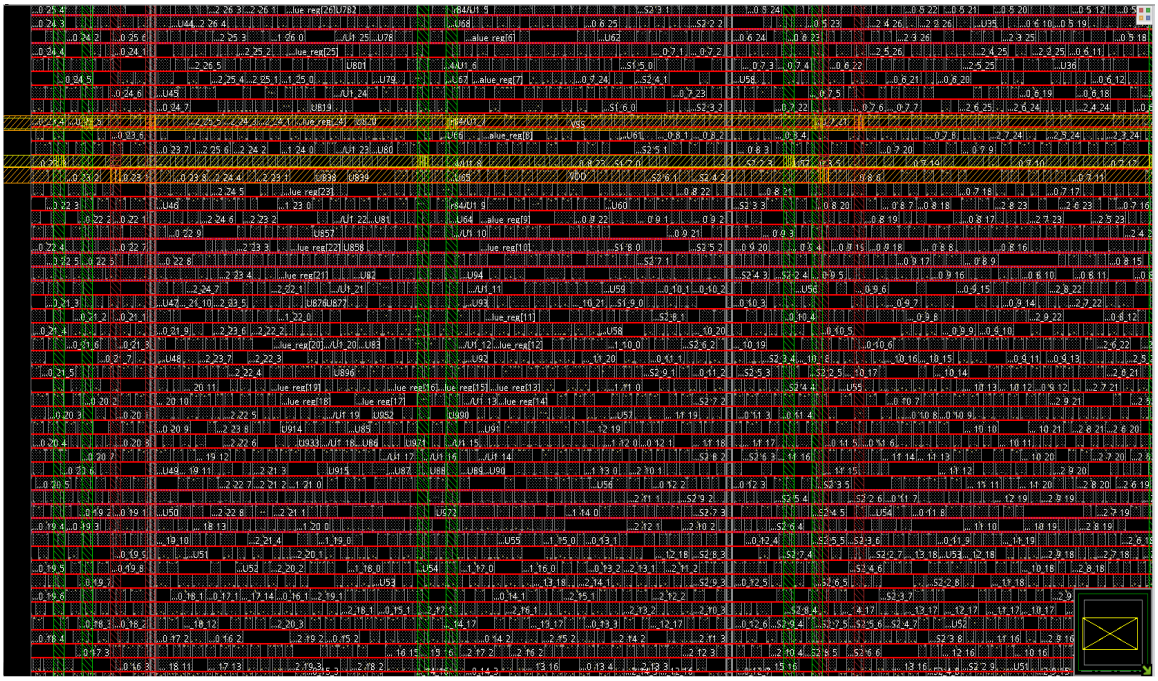

Fig. 6.6. Placement of the standard cells.

tools is to use core area efficiently and provide enough space for signal routing. The placed standard cells are depicted in Figure 6.6.

6.6.3 Clock Tree Synthesis

In modern systems, the performance is directly proportional to its clock frequency. Clock nets need to be routed on higher metal layers to avoid reliability issues. This is achieved by designing them with great precision. There are multiple clock methodologies are for clock implementation such as H-tree and Clock-tree mesh. All methodologies use clock repeaters in the clock path to avoid distortion in the clock signal. As the clock is one of the high activity net on-chip, the clock router needs to include the resistance and capacitance of the metal layers, the noise glitch and cross talk in parallel running interconnects, and the driving load while routing them [51].

6.6.4 Routing

Routing algorithms are mainly classified as channel or feed-through based routers. These algorithms perform routing in three steps: Global routing, Track assignment, and Detailed routing. Global routing deals with the creation of global route cells. After the global route estimation is completed, all the metals are assigned with the available tracks in that GRC. The detailed routing deals with the actual layout of the metal interconnect for the assigned metal layer. Modern semiconductor processes utilize more than 10 metal layers in technology specification that increases the number of routing tracks and its density in the core area. Each place and route tool comes with advanced inbuilt routers and are utilized for high-performance cross-talk aware routing. Cadence Innovus uses NanoRouter for its design and based on advanced routing techniques to route the design with minimum wire length [19]. The routed cell and design are shown in Figure 6.7. The post routing power is calculated on Innovus. Internal power, switching power, and leakage power are reported to be 2705 mW, 7599 mW, and 0.00743 mW respectively. The clock tree power is the most active net of a design and has huge power consumption as compared to other nets in the design. In this design, the power is found to be 87.86mW which shows the efficiency of the 7nm FinFET design.

6.6.5 Final Layout

The post-routed design of the ALU is depicted figure 6.8. This design contains all the standard cell abstract physical views with the interconnects connecting them. Apart from the routes, the cell coordinates, orientation, metal tracks, via locations and PG net shapes can be written out in design exchange format (DEF). The abstract view contains the pins information of the cells and can be seen by streaming-in the GDSII format in Cadence Virtuoso Layout XL tool. The interconnect parasitic format can be extracted to perform further timing and physical verification of different tools as a part of future work.

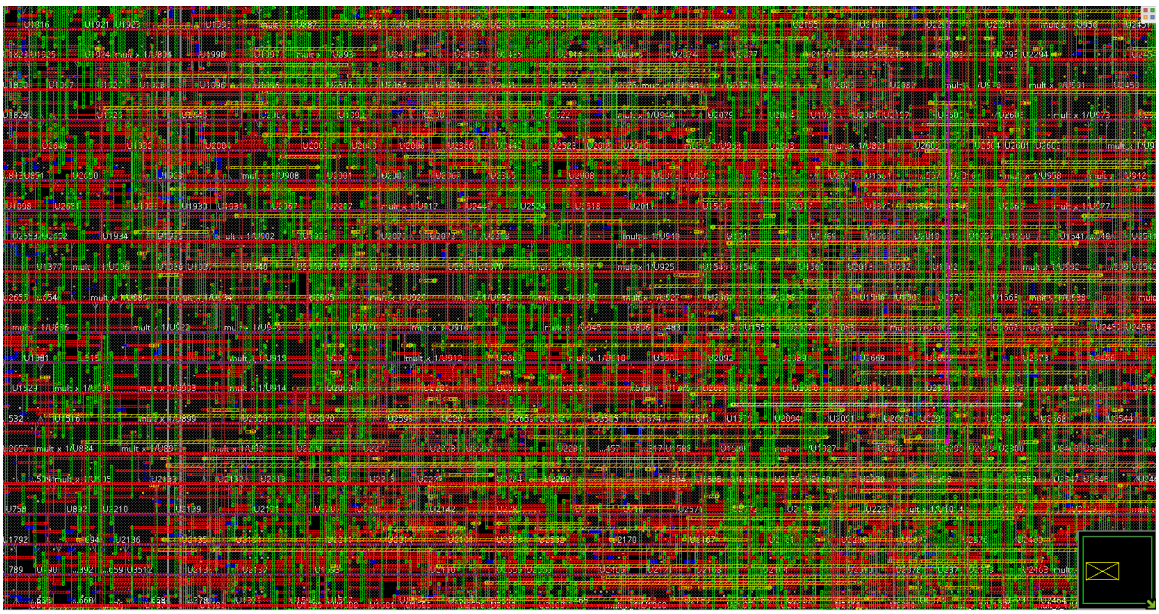

Fig. 6.7. Routing.

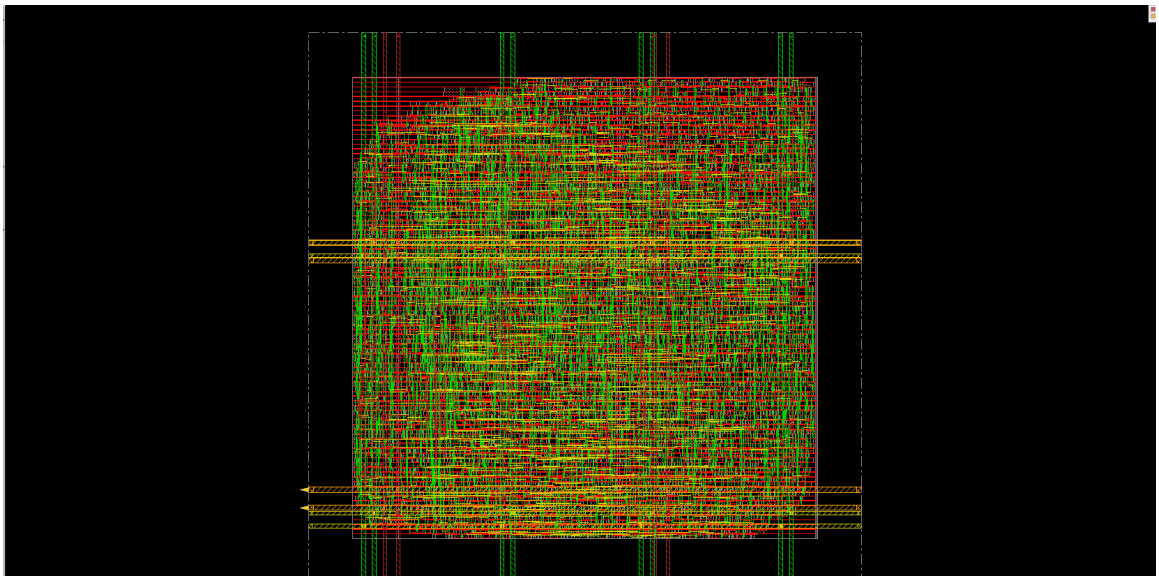

Fig. 6.8. Layout of the ALU design.

7. RESULTS AND DISCUSSION

In this thesis, the 7nm FinFET designs were successfully implemented using custom and digital design methodologies. The implementation was done on different tools. For custom design methodology, spectre simulator was utilized with the Analog Design Environment (ADE) Explorer and Assembler. The digital design methodology uses multiple tools from different vendors. A design methodology was developed to integrate the Synopsys front-end and Cadence back-end tools. The designs were proposed for various applications with power, performance, and area as a figure of merits.

The 7nm NMOS transistor was characterized on Cadence Virtuoso for the threshold voltage, gate capacitance, effective current, dissipated power, subthreshold leakage current, and the subthreshold slope. The minimum slope was achieved to be 62 mV/decade that shows its leakage control capability over other accessible silicon transistor models. In modern SoCs, clock distribution is one of the most challenging parts of the design implementation. It considers the effect of variability, minimum pulse width requirement, latencies, and skews. The clock repeaters need to provide symmetry for every rise and fall transitions. This thesis proposes a clock inverter that can be used efficiently without balancing PMOS and NMOS width. Further, the sizing problem for the optimized stage effort was also accounted for by characterizing the FO6 delay for the nonlinear delay model and composite current source timing models. The 7nm ASAP library also comes with the special SRAM transistors that are considerably high threshold voltage transistor models. This thesis presents the characterization of SRAM Vt inverter cell for the power and effective current that shows the VTC of an individual cross-coupled inverter. The functionality of 6T SRAM was also verified with the multi-corner analysis of read and write noise

margin for robustness. The static noise margin for read and write operation was also compared for the different threshold voltage transistors.

To assess the robustness of the library further, a system-level design was also presented that was synthesized on different operating conditions. The implementation was executed using the digital design methodology. The design was also checked for formal verification for logic equivalence check on Synopsys Formality. In the physical implementation part, the design was imported on Cadence Innovus for automatic place & route. The design proposes a 32-bit ALU for the complex computational application on 1 GHz clock frequency and can be instantiated as a soft or hard IP in integer execution units of the ASIC system.

8. CONCLUSION AND FUTURE WORK

The 7nm library characterizes circuits and systems efficiently to achieve enough robustness for good power, delay, and area QoRs.

The variability can be estimated using probabilistic approaches. Advanced techniques like On-Chip Variation, Advance On-Chip Variations, and Parametric On-Chip Variation can be added to the library with Liberty Variation Format (LVF) to increase the robustness significantly [52]. These approaches are part of statistical approximation for delay calculation. The presented design in this dissertation covers from SS to FF corners, which usually covers from -3σ to +3σ on a Gaussian statistical distribution. The overall rejection rate for this approach is 0.26%. That means if the number of transistors is 1 billion, the 2.6 million will get affected by the variation and may not perform at the desired speed. The real-world designs are closed on 4-5σ to achieve phenomenal robustness. However, memory designs are highly dense and require timing sign-off at 7-8σ to perform desirably at the worst possible condition. This robustness can be achieved by considering statistical modeling of timing variation with the LVF file and it is reserved as a part of future work.

REFERENCES

REFERENCES

[1] M. Taylor *et al.*, "Asic clouds: Specializing the datacenter for planet-scale applications," *Communications of the ACM*, pp. 103–109, 2020.

[2] M. C. and S. C., *Algorithms and Heuristics in VLSI Design*, 1st ed. Springer, Berlin, Heidelberg, 2002.

[3] N. Jouppi, C. Young, N. Patil, and D. Patterson, "Motivation for and evaluation of the first tensor processing unit," *in IEEE Micro*, pp. 10–19, 2018.

[4] N. P. J. et al., "In-datacenter performance analysis of a tensor processing unit," *in 2017 ACM/IEEE 44th Annual International Symposium on Computer Architecture (ISCA)*, pp. 1–12, 2018.

[5] D. Etiemble, "45-year cpu evolution: one law and two equations," *in Second Workshop on Pioneering Processor Paradigms*, pp. 1–6, 2018.

[6] Y. L. et al., "Performance of stacked nanosheets gate-all-around and multi-gate thin-film-transistors," *in IEEE Journal of the Electron Devices Society*, pp. 1187–1191, 2018.

[7] V.Vashishtha, L.T.Clark, D.M.Harris, S.Dietrich, and Z.Wang, "Design flows and collateral for the asap7 7nm finfet predictive process design kit," *in 2017 IEEE International Conference on Microelectronic Systems Education (MSE)*, pp. 1–4, 2017.

[8] L. T. Clark, V. Vashishtha, L. Shifren, A. Gujja, S. Sinha, B. Cline, C. Ramamurthy, and G. Yeric, "Asap7: A 7-nm finfet predictive process design kit," *in 2016 Microelectronics Journal*, pp. 105–115, 2016.

[9] B. T. Geetha, B. Padmavathi, and V. Perumal, "Design methodologies and circuit optimization techniques for low power cmos vlsi design," *in2017 IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI)*, pp. 1759–1763, 2018.

[10] C. D. Systems, "Cadence quantus extraction solution user guide," vol. 19.00, 2019.

[11] V.Vashishtha, A.Dosi, L.Masand, and L.T.Clark, "Design technology co-optimization of back end of line design rules for a 7 nm predictive process design kit," *in 2017 18th International Symposium on Quality Electronic Design (ISQED)*, pp. 149–154, 2017.

[12] Synopsys, "Liberty user guides and reference manual," vol. Version 2014.09, 2014.

[13] J. Liu, J. Zeng, A. Hong, L. Chen, and C. C. P. Chen, "Process-variation statistical modeling for vlsi timing analysis," *in 9th International Symposium on Quality Electronic Design (isqed 2008)*, pp. 730–733, 2008.

[14] X. Zhang, K. Ishida, H. Fuketa, M. Takamiya, and T. Sakurai, "On-chip measurement system for within-die delay variation of individual standard cells in 65-nm cmos," *in IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, pp. 1876–1880, 2012.

[15] M. Huang and M. A. Styblinski, "An approach to vlsi circuit reliability optimization considering the hot electron effects," *in 1992 IEEE International Symposium on Circuits and Systems*, pp. 1101–1104, 1992.

[16] C. P. et al, "Dielectric breakdown in a 45 nm high-k/metal gate process technology," *in 2008 IEEE International Reliability Physics Symposium*, pp. 667–668, 2008.

[17] J. Choi, S. Lee, J. Paik, and Y. Joo, "Electromigration behavior of eutectic snpb solder," *in Advances in Electronic Materials and Packaging 2001*, pp. 417–420, 2001.

[18] V. Vashishtha, M. Vangala, P. Sharma, and L. T. Clark, "Robust 7-nm sram design on a predictive pdk," *in 2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–4, 2017.

[19] C. D. Systems, "Innovus user guide," vol. Version 19.10, 2019.

[20] SynopsysDP, "Ic compiler 2 design planning user guide," vol. Q-2019.12, 2019.

[21] SynopsysTiming, "Synopsys ic compiler 2 timing analysis user guide," vol. Q-2019.12, 2019.

[22] SynopsysICC2, "Ic compiler 2 implementation user guide," vol. Q-2019.12, 2019.

[23] SynopsysCCS, "Ccs timing library characterization guidelines," vol. Version 3.4, 2016.

[24] SynopsysDC, "Deisgn compiler user guide," vol. Q-2019.12, 2019.

[25] SynopsysLC, "Library compiler user guide," vol. Q-2019.12, 2019.

[26] C. Mack, "The multiple lives of moore's law," *in IEEE Spectrum*, pp. 31–31, 2015.

[27] B. Y. et al, "Finfet scaling to 10 nm gate length," *in Digest. International Electron Devices Meeting*, pp. 251–254, 2002.

[28] L. C. et al., "The multiple lives of moore's law," *in IEEE Circuits and Devices Magazine*, pp. 35–42, 2003.

[29] N. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed. Pearson, 2010.

[30] A. Chandrakasan and W. J. Bowhill, *Design of High-Performance Microprocessor Circuits*, 1st ed. Wiley-IEEE, 2001.

[31] N. P. et al., "Bsim—spice models enable finfet and utb ic designs," *in IEEE Access*, pp. 201–215, 2013.

[32] C. Auth, "22-nm fully-depleted tri-gate cmos transistors," *in Proceedings of the IEEE 2012 Custom Integrated Circuits Conference*, pp. 1–6, 2012.

[33] C. Wu, D. Lin, A. Keshavarzi, C. Huang, C. Chan, C. Tseng, C. Chen, C. Hsieh, K. Wong, and M. Cheng, "High performance 22/20 nm finfet cmos devices with advanced high-k/metal gate scheme," *in Proceedings of the IEDM*, pp. 27.1.1–27.1.4, 2008.

[34] S. Sinha *et al.*, "Circuit design perspectives for ge finfet at 10 nm and beyond," *in Proceedings of the ISQED*, pp. 57–60, 2015.

[35] A. Pyzyna *et al.*, "Resistivity of copper interconnects beyond the 7 nm node," *in VLSI Technology Symposium Digest of Technical Papers*, pp. T120–T121, 2015.

[36] J. H. Chen, T. E. Standaert, E. Alptekin, T. A. Spooner, and V. Paruchuri, "Interconnect performance and scaling strategy at 7 nm node," *in IEEE International Interconnect Technology Conference*, pp. 93–96, 2014.

[37] P. J. Restle and A. Deutsch, "Designing the best clock distribution network," *in 1998 Symposium on VLSI Circuits. Digest of Technical Papers*, pp. 2–5, 1998.

[38] F. E. Anderson, J. S. Wells, and E. Z. Berta, "The core clock system on the next-generation ltaniumlm microprocessor," *in 2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, pp. 110–424, 2002.

[39] N. A. Kurd, J. S. Barkarullah, R. O. Dizon, T. D. Fletcher, and P. D. Madland, "A multigigahertz clocking scheme for the pentium(r) 4 microprocessor," *in IEEE Journal of Solid-State Circuits*, pp. 1647–1653, 2001.

[40] S. Kang and Y. Leblebigi, *Design of High-Performance Microprocessor Circuits*, 3rd ed. McGraw-Hill, 2003.

[41] A. J. Bhavnagarwala, X. Tang, and J. D. Meindl, "The impact of intrinsic device fluctuations on cmos sram cell stability," *in IEEE Journal of Solid-State Circuits*, pp. 658–665, 2001.

[42] H. Bhatnagar, *Adavanced ASIC Chip Synthesis*, 2nd ed. Kluwer Academic, 2002.

[43] A. J. de Geus, "Logic synthesis speeds asic design," *in IEEE Spectrum*, pp. 27–31, 1989.

[44] SynopsysHDL, "Hdl compiler for verilog user guide," vol. 2019.12, 2019.

[45] SynopsysSDC, "Synopsys design constraint application notes," vol. 2.1, 2017.

[46] Cypress, "Jitter in pll-based systems: Causes, effects, and solutions," 2011.

[47] SynopsysPT, "Synopsys primetime user guide," vol. Q-2019.12, 2019.

[48] SynopsysF, "Formality user guide," vol. Q-2019.12, 2019.

[49] N. Sherwani, *Algorithms for VLSI Physical Design Automation*, 1st ed., 1996.

[50] F. H. N. Xu and Z. Jiang, "A fast algorithm for vlsi building blockplacement," *in The Proceedings of the Multiconference on "Computational Engineering in Systems Applications"*, pp. 2157–2160, 2006.

[51] G. .Wu, S. Jia, Y. Wang, and G. Zhang, "An efficient clock tree synthesismethod in physical design," *in 2009 IEEE International Conference ofElectron Devices and Solid-State Circuits (EDSSC)"*, pp. 190–193, 2009.

[52] SynopsysLVF, "Liberty variation format," vol. Version 2017.06, 2017.